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A Simple On-Chip Automatic Tuning Circuit for Continuous-Time Filter

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Abstract

A simple on-chip automatic frequency tuning circuit is proposed. The tuning circuit is modified from voltage-controlled filter (VCF) frequency tuning circuit. We utilize an operational transconductance amplifier and a capacitor to from a single-time constant (STC) circuit which can produce a controllable delay time clock to tune the frequency of the filter. It can efficiently reduce the deviations in the 3 dB bandwidth from the variations of PVT (Process, Voltage and Temperature). The design of the STC circuit is simpler than VCF and it has less chip area. The chip has been implanted using TCMC 0.35 μm CMOS technology and the power consumption is less than 9.05 mW.

Keywords: Automatic, Tuning, Voltage-Controlled Filter (VCF), Single-Time Constant (STC)

1. Introduction

Analog continuous-time filters [1] are popular in various application, such as video and audio signal processing, ADC, mobile phone, hard disk reading channels, CD- ROM, etc. Recently, the Gm-C filters are widely used in the CMOS technology. The Gm-C filters have higher frequency and flexibility than other analog filter types. However, their performances vary with process and environment variations. The frequency response of analog continuous-time filters is determined by resistors, capacitors or transconductors. However, the process variation, temperature drift and aging, make the integrated RC time constants vary about 30% [2,3]. At extreme conditions, the maximum frequency response deviations could be up to 50% [4]. To achieve the desired filter performance, an on-chip automatic tuning scheme is usually required [5–14].

Many kinds of frequency automatic-tuning methods are derived from phase locked loop (PLL) for analog filters, such as sinusoidal oscillator based PLL tuning circuit, voltage-controlled filter (VCF) tuning circuit and etc [1,5,6,13]. The drawbacks of the sinusoidal oscillator based PLL tuning are large size and hard to design. As to the voltage-controlled filter tuning circuit, the power consumption is high and the reference clock needs to be a pure sine wave. According to the aforementioned, we try to make the tuning circuit have following advantages: simplicity, small chip area, good matching with the filter and less power consumption.

In the following sections, Section 2 presents the proposed tuning circuit and the Gm-C filter and the experimental results are discussed in Section 3. Section 4 summarizes the conclusions of this paper.

2. The Proposed Tuning Circuit and the Gm-C Filter

2.1. The Operation of Proposed Tuning Mechanism

Figure 1 shows the proposed tuning circuit scheme. Firstly, the frequency tuning circuit is modified from voltage-controlled filter (VCF) frequency tuning circuit. We replace VCF by a single-time-constant (STC) circuit and the input signal could be square wave. The function of STC is to produce a delay clock which the delay can be controlled. The phase difference will make the charge pump (CP) produce a control voltage. The phase difference is 45° between the reference clock and the output of the voltage comparator. The tuning circuit depends on the constant phase difference to tune the slave filter. Finally, it generates the control voltage after the voltage signal is filtered by the low pass filter (LPF).

Next, we discuss the STC circuit. The STC circuit consists of a tunable OTA, as shown in Figure 2, and a capacitor. We use the tunable OTA to simulate a variable resistance, and we obtain a STC circuit by connecting the OTA with a capacitor.

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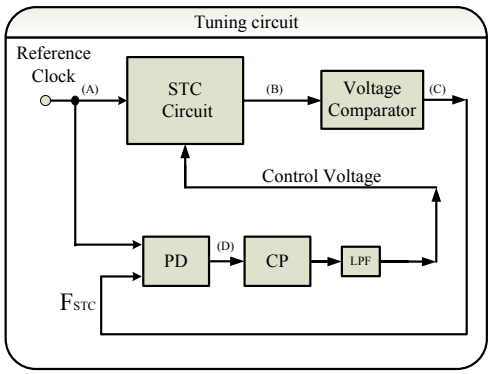

Figure 1. The block diagram of tuning circuit. (PD: Phase Detector, CP: Charge Pump, LPF: Low Pass Filter).

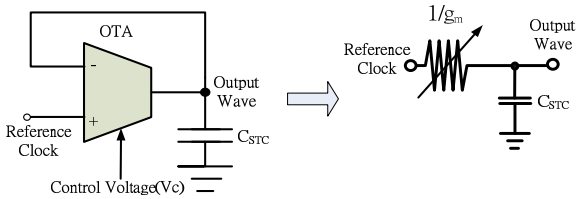

Figure 2. The STC circuit.

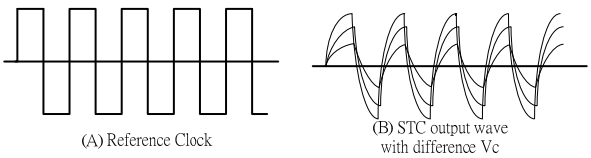

Figure 3. (A) Reference clock (B) STC output wave with three different Vc.

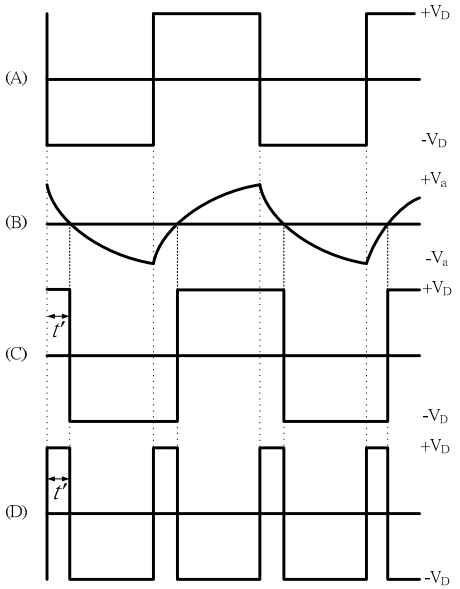

Figure 4. (A) Reference clock (B) The output of the STC circuit (C) The output of the voltage comparator (D) The output of the PD.

The transfer function of the STC is

$$T(s) = \frac{1}{1+\frac{s}{w_0}} \tag{1}$$

$$w_0 = \frac{1}{\tau} = \frac{1}{RC} = \frac{gm}{C}. \tag{2}$$

If we input a reference clock, the STC will output a pseudo-triangular wave. The output wave of the STC circuit with three different control voltages V_c are shown in Figure 3.

When we input a reference clock with amplitude ± V_D as shown in Figure 4(A), the STC circuit will output a pseudo-triangular wave with amplitude ± V_a as shown in Figure 4(B). The pseudo-triangular wave is symmetrical with respect to the zero voltage. We will use a voltage comparator which is referenced at the zero voltage, so it will produce a clock with a delay time, t', as shown in Figure 4(C). We can find out the relation between the delay time and the time constant, τ, of the pseudo-triangular wave.

From Figure 4(B), it can be derived that the relation between t' and τ is:

$$\frac{t'}{T} = \frac{\ln(\frac{2}{1+e^{-T/2\tau}})}{\frac{T}{\tau}} \tag{3}$$

$$f_o = \frac{1}{2\pi\tau} = \alpha f_{clock} \qquad \alpha = \frac{T}{2\pi\tau} \tag{4}$$

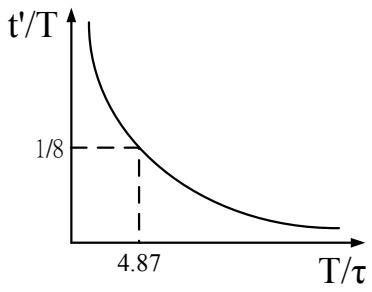

Figure 5. t'/T VS T/τ.

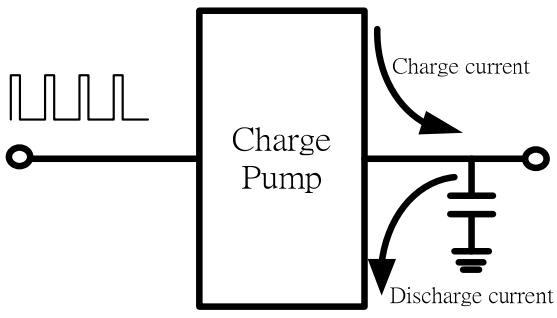

Figure 6. Charge and discharge current.

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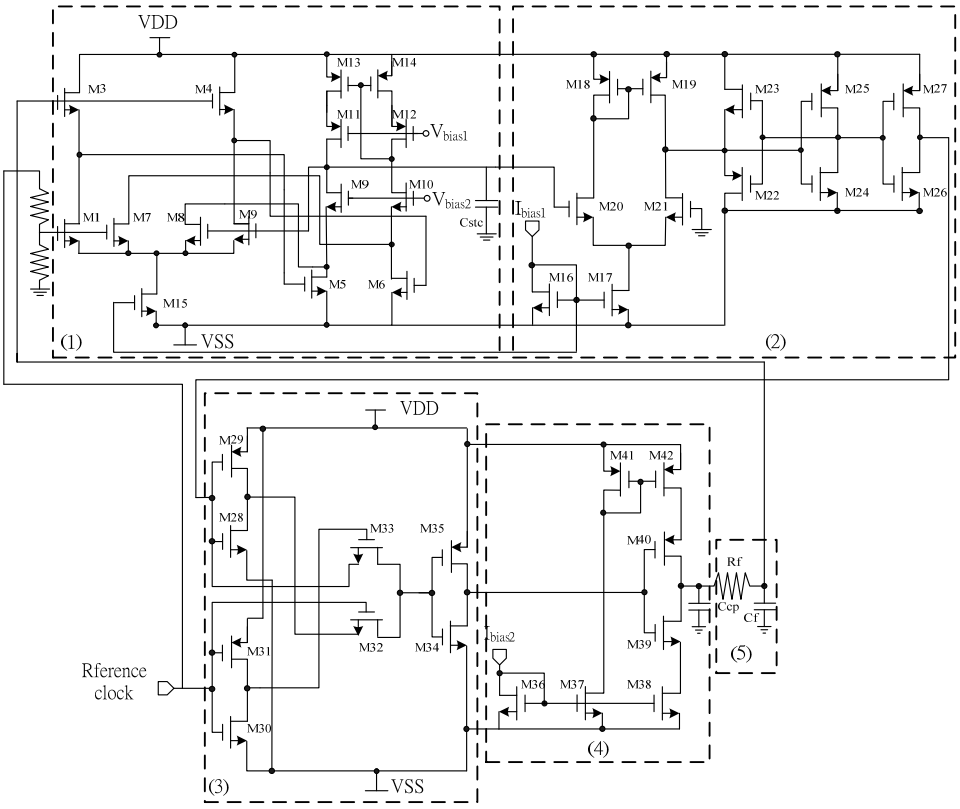

Figure 7. The structure of proposed tuning circuit ((1): STC circuit, (2): Voltage comparator, (3): Phase Detector, (4): Charge Pump, (5): Low Pass Filter).

Figure 5 is the curve of Equation (3). If we choose t'/T = 1/8, then α = 0.776. When T = 10MHz, the critical frequency of the STC is 7.76MHz.

Figure 6 shows a diagram of the charge and discharge current in CP. We set the charge current and discharge current with a ration 3:1. At charge balance, the reference frequency and STC output will be locked at 45° phase difference such that t'/T = 1/8. For the other, we adjust the delay time of the STC with a constant reference clock. The STC circuit is transferred to a square wave, as shown in Figure 4(C). We will detect the phase difference of two square waves by a phase detector, as shown in Figure 4(D). This wave is applied to the charge pump to adjust τ, as shown in Figure 6. At the output of the charge pump, the charge current is three times the discharge current. Because of electric balance, the delay time will be T/8.

2.2. The Structure of Proposed Tuning Circuit

Figure 7 shows the proposed circuit that is consisted of five sub circuits. The first part of the proposed circuit is the STC circuit. It consists of a tunable OTA [8] and a capacitor. We can find the transconductance of the OTA is:

$$gm = 2k(V_c - 2V_T) \tag{5}$$

where $k=0.5\mu_n C_{ox}W/L$ is the transconductance parameter, and $\mu_n C_{ox}W$ and L are the mobility, oxide capacitance per unit area, channel width and length, respectively. V_T is the threshold voltage, and V_c is the OTA's control voltage. We can adjust the STC's RC time by varying the OTA's control voltage, V_c. It stands to reason that the tunable OTA's design is easier than a VCF and the size is much smaller than a VCF. When the Reference Clock is applied to the STC circuit, a differential pseudo-triangular wave will be produced. If the control voltage is higher, the g_m will be bigger. The charge and discharge

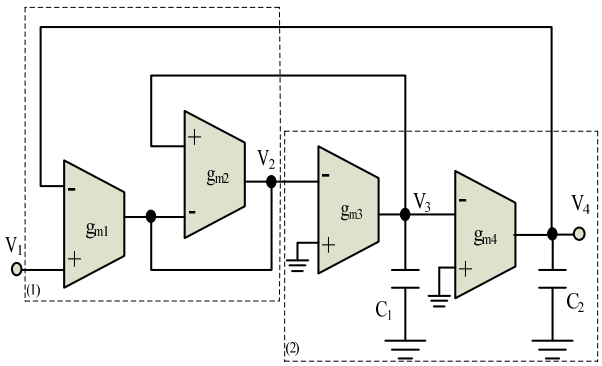

Figure 8. Two-order Gm-C biquad filter [12].

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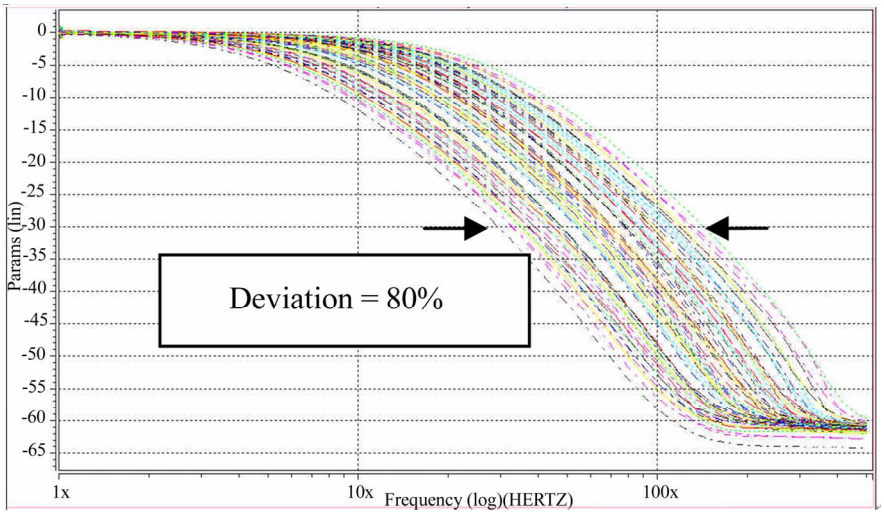

Figure 9. The 3-dB frequency variation in sixty corners (without tuning).

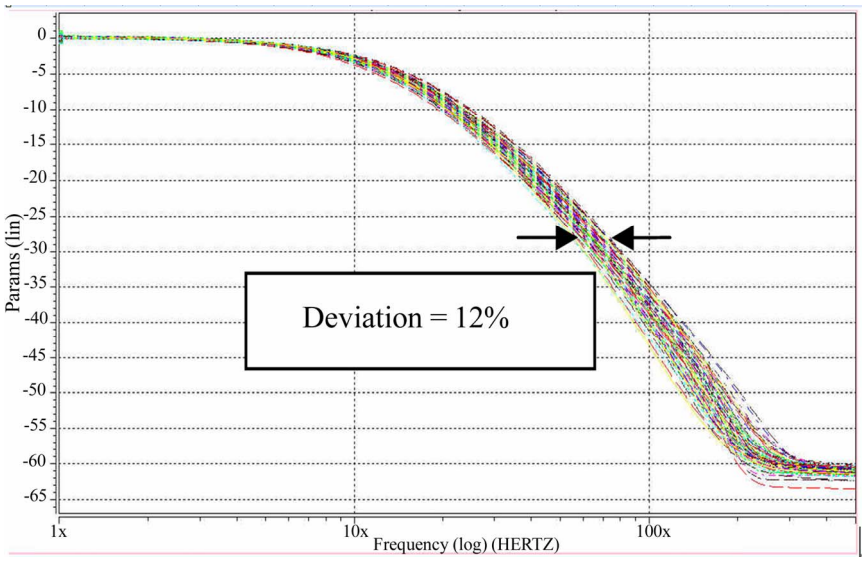

Figure 10. The 3-dB frequency variation in sixty corners (with tuning).

of the capacitor will be quicker. The phase difference between the output wave and the reference frequency will be smaller. Finally, the phase difference will be locked at the specified value.

The voltage comparator is composed of a V-I converter, a current comparator and an inverter, as shown in Figure 7(2). The delay of the voltage comparator is longer than the sum of these devices' delay and the sum of these devices' delay is shorter than a conventional high speed voltage comparator. Next, we want to detect the phase difference between the reference frequency and the output wave of the Inverter. We use a phase detector, which is constructed by an XNOR, as shown in Figure 7(3). Figure 7(4) is the charge pump (CP). The capacitor will be charged and discharged by current source. M36,M37, M38, M41 and M42 are three current mirrors. M37 and M38 will mirror M36's current I_{bias} and $I_{discharge}$ is equal to I_{bias} because M42's size is almost three times as M41. I_{charge} is equal to $3I_{bias}$. We set the charge current and discharge current with a ratio 3:1. At charge balance, the reference frequency and STC output will be locked at 45° phase difference. If the current source of the CP is large, the phase will be quickly locked. But the ripple will be large. To reduce the ripple, we use a low-pass filter (LPF) like in Figure 7(5).

2.3. The Gm-C Filter

Figure 8 shows a two-order Gm-C low-pass filter made by OTAs [12]. The cut-off frequency is 10 MHz by design. We will use this filter to prove our tuning circuit is working. The transfer function can be expressed as:

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$$\frac{V_4}{V_1} = \frac{\omega_o^2}{s^2 + (\omega_o / Q)s + \omega_o^2} \quad (6)$$

where $\omega_o = \sqrt{\frac{g_{m1}g_{m3}g_{m4}}{g_{m2}C_1C_2}}$ and $Q = \sqrt{\frac{g_{m1}g_{m4}C_1}{g_{m2}g_{m3}C_2}}$.

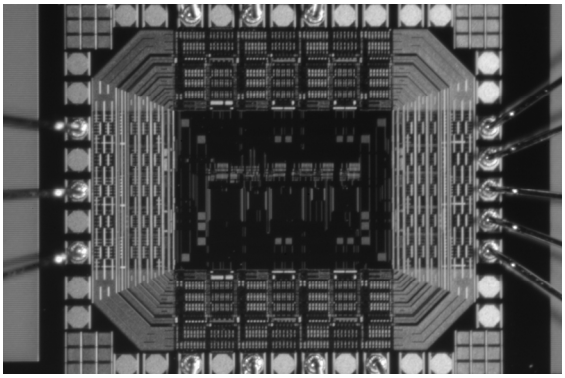

Figure 11. Die photo of the proposed circuit.

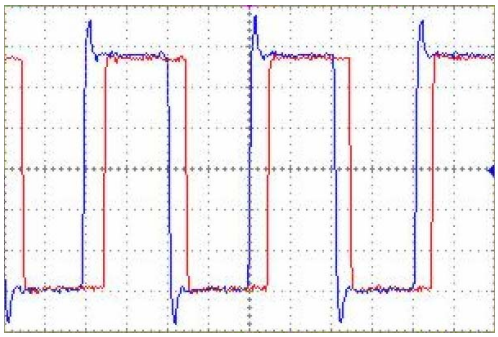

Figure 12. Reference clock and delay clock.

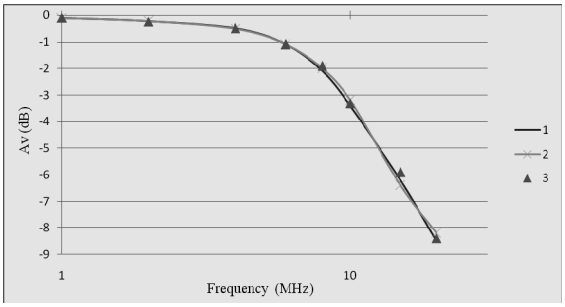

Figure 13. Filter frequency responses in three samples.

Table 1. Filter performance parameter.

Technology	TSMC 0.35μm CMOS
Supply Voltage	±1.5 V
Chip area	1477 μm x 1267 μm
3-dB bandwidth	9.5~9.6 MHz
Reference clock	10 MHz
Power consumption	< 9.05 mW
Tuning error	<12.0%

3. Simulation and Experimental Results

The simulation is carried out using HSPICE with TSMC 0.35um CMOS models. There are five modes of SPICE model, TT, FF, SS, FS and SF. These five models are used to simulate the CMOS process variation. Figure 9 shows the 3-dB frequency variation in sixty corners. The sixty corners include five CMOS models(TT、FF、SS、FS、SF), three voltages (±1.35 V、±1.5 V、±1.65 V) and four temperatures (-20℃, 0℃, 25℃, 70℃).

Without the tuning circuit, the maximum variation of the 3-dB frequency in sixty corners is about 80%.

Figure 10 shows the simulation result of the low-pass Gm-C filter with the tuning circuit in sixty corners. The maximum variation of the 3-dB frequency in sixty corners is about 12%. Comparing Figure 9 with Figure 10, we find that the frequency tuning circuit can reduce 3-dB frequency variation from 80% to 12%.

The proposed circuit is implemented by 0.35 μm TSMC 2P4M CMOS process and its die photograph is shown in Figure 11. The chip area is 1477 μm x 1267 μm. We have measured the delay clock to check if the tuning circuit operates correctly. Then we measure filter output to check the bandwidth. Figure 12 shows reference clock and delay clock. Figure 13 shows the filter frequency response in three samples.

The measured performance of the filter are shown in Table 1. The performance of the proposed circuit was good, confirming the expectation that the tuning circuit can reduce the tolerance. Also the power consumption is small and less than 9.05 mW.

4. Conclusions

This paper has presented a simple automatic tuning circuit, which is applied to a ± 1.5 V 10 MHz low-pass Gm-C filter. The greatest advantage of the proposed tuning circuit is compact and easy to be realized without designing a complicated voltage controlled oscillator. The size of the tuning circuit is another advantage. The chip area is only about 0.12 x 0.14 mm^2. From the results, the frequency tuning circuit can reduce the frequency tolerance efficiently. All the circuits are designed based on the TSMC 0.35 μm 2P4M CMOS process technology.

5. Acknowledgment

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