

A Novel Packet Switch Node Architecture for Contention Resolution in Synchronous Optical Packet Switched Networks

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ABSTRACT

Packet contention is a key issue in optical packet switch (OPS) networks and finds a viable solution by including optical buffering techniques incorporating fiber delay lines (FDLs) in the switch architecture. The present paper proposes a novel switch architecture for packet contention resolution in synchronous OPS network employing the packet circulation in FDLs in a synchronized manner. A mathematical model for the proposed switch architecture is developed employing packet queuing control to estimate the blocking probability for the incoming traffic. The switch performance is analyzed with a suitable contention resolution algorithm through the computer simulation. The simulation results substantiate the proposed model for the switch architecture.

Keywords: Fiber Delay Lines, Packet Circulation, Optical Packet Switch Networks, Packet Delay Probability, Contention Resolution.

1. Introduction

The growth of optical transmission technology in recent years is significant by achieving a Tbps class of transmission speed. However, a rapid increase in the bandwidth requirement for optical network to support high data rate puts the switching speed limit for the supporting electronic technology. Thus, we need a photonic network which can incorporate functions such as the multiplexing, de-multiplexing, switching, and routing in the optical domain substituting the electronic control circuitry. A number of research groups have reported various optical sub-wavelength switching approaches [1-3] and OPS approach [4,5] attracts attention as it is capable of dynamically allocating network resources with fine granularity and excellent scalability. In general, packet switch optical networks can be divided into two categories: synchronous networks with fixed length packets and asynchronous networks with fixed size or variable-size packets. In an OPS network, contention occurs at a switching node whenever two or more packets try to leave the switch fabric on the same output port, on the same wavelength, at the same time. This is a problem

that commonly arises in packet switches, and is known as external blocking. Techniques used to address this problem include optical buffering, wavelength conversion and deflection routing.

Usually in a contention resolution method, wavelength conversion is a superior option as it does not introduce delay in the data path and also avoid packet re-sequencing. On the other hand number of converters and placement of these converters in the network is NP complete problem [6,7]. The deflection routing exploits the space dimension to resolve contention. It introduces delays in the data path and requires packet re-sequencing as packets may arrive out of order. This makes deflection routing not a good choice as contention resolution [8].

Optical buffering is fundamental to many optical packet switch implementation which have been proposed widely to overcome contention problem [9,10]. One of the contending packets is routed through the switch fabric, while the rest are sent to FDLs. Optical buffers may be placed at the input, output, or both, in a switch. However, a number of optical buffer arrangements have been proposed in the literature, such as single or multi-stage FDLs, feed-forward or feed-backward connections. [11-14]

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These three contention resolution schemes have been used in pure form, or they combined to implement more sophisticated strategies. Each of these arrangements is used to implement a variety of packet switch architectures [15–18]. These schemes, along with the various combinations, make possible a wide spectrum of contention resolution methods that cover various tradeoffs of performance versus cost and complexity.

It is observed that the existing buffering implementations require a huge amount of FDLs as well as complex switch architecture that increases the overall cost of the switch. In particular, switch architecture designed in [13] uses a single level of FDLs i.e. all buffers are in shared mode. This model performance degrades with the rise in arriving packet rate or requires more delay lines to reduce blocking probability. The switch hardware cost can be better managed with a proper node architecture design with a better contention resolution scheme involving flexible delay lines. This design can be further modified to allow packet circulation in buffers or FDLs. This paper proposed a switch architecture that utilizes the delay lines in efficient way involving packet circulation to resolve the contention. The proposed node architecture is presented along with a contention resolution algorithm in Section 2.

2. Node Architecture and Contention Resolution Algorithm

Proposed node architecture consists of k fixed length FDLs labeled as f_1, f_2, \dots, f_k each having delay length similar to packet transmission time to keep synchronization. Conflicted packets are circulated in the FDLs causing delay in multiples of T and makes nT time unit delay after n loop circulation. In case of contention for a particular output port let say m , one packet is transmitted to the desired output port and remaining packets are diverted to the fixed sized free FDLs as per the proposed algorithm.

Additional output ports are connected to the switch through FDL lines as shown in Figure 1. The appropriate FDL lines are chosen through the feedback control mechanism to resolve the packet contention. If two

packets (packet-1 and packet-2) are competing for same output port m at time t_0 , the packet-1 can be send to the desired output port and the packet-2 is send to one of the free FDL at time t_1 as decided by the FDL control system. The packet-2 is emergence from the delay line at time t_2 ; simultaneously packet-1 is transmitted successfully at time t_2 from output port m . Now this port is free to send packet-2 at time t_3 . Let us say at time t_3 a new packet (packet-3) competes for port m then packet-2 and packet-3 are in contention with delay time T and 0 respectively. Now packet-3 is send to one of the free FDL and packet-2 will be directed towards the desired output port. Here scheduling algorithm based on delay time is developed to divert the packets in appropriate direction. The packets can be delayed through FDL control up to desired amount of time by circulation. Maximum possible delay time is decided by the signal to noise ratio at the output port which depends upon fiber characteristics. Eventually this constraint limits the number of maximum possible circulation for a given packet with in the FDL structure. The overall performance of the system is improved as circulation frequency is increased that compensate the additional cost involved for the switch. The description of the proposed algorithm is illustrated through a flow chart as shown in Figure 2.

A control structure, maintained inside the control block of the switch keeps track of the status (0 for free and 1 for used) of the each delay line, contended output port (output port number from which packet belongs) and delay time (how long packet is delayed). A mathematical model has been developed to visualize the internal behavior of the proposed switch architecture. The model involves auxiliary FDLs to resolve the packet contention and it is based on Erlang B data traffic model having data arrival rate and packet transmission time as λ and $1/\mu$ respectively. Here each fiber consisting of W channels.

Consider an output fiber say F , of the switch, we assume S sources sending optical packet traffic destined for fiber F . Let the on and off periods of each source be exponentially distributed with common means $1/\sigma$ and $1/\tau$, respectively. The mean offered load (ρ) to the system is given in [10]:

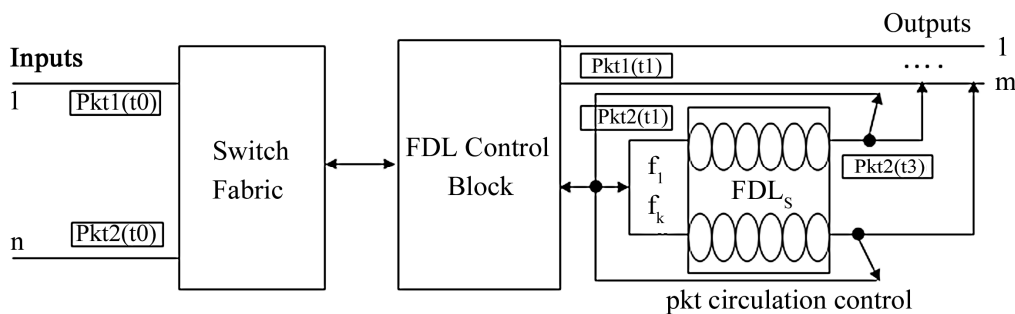


Figure 1. Proposed Packet Switch Node Architecture.

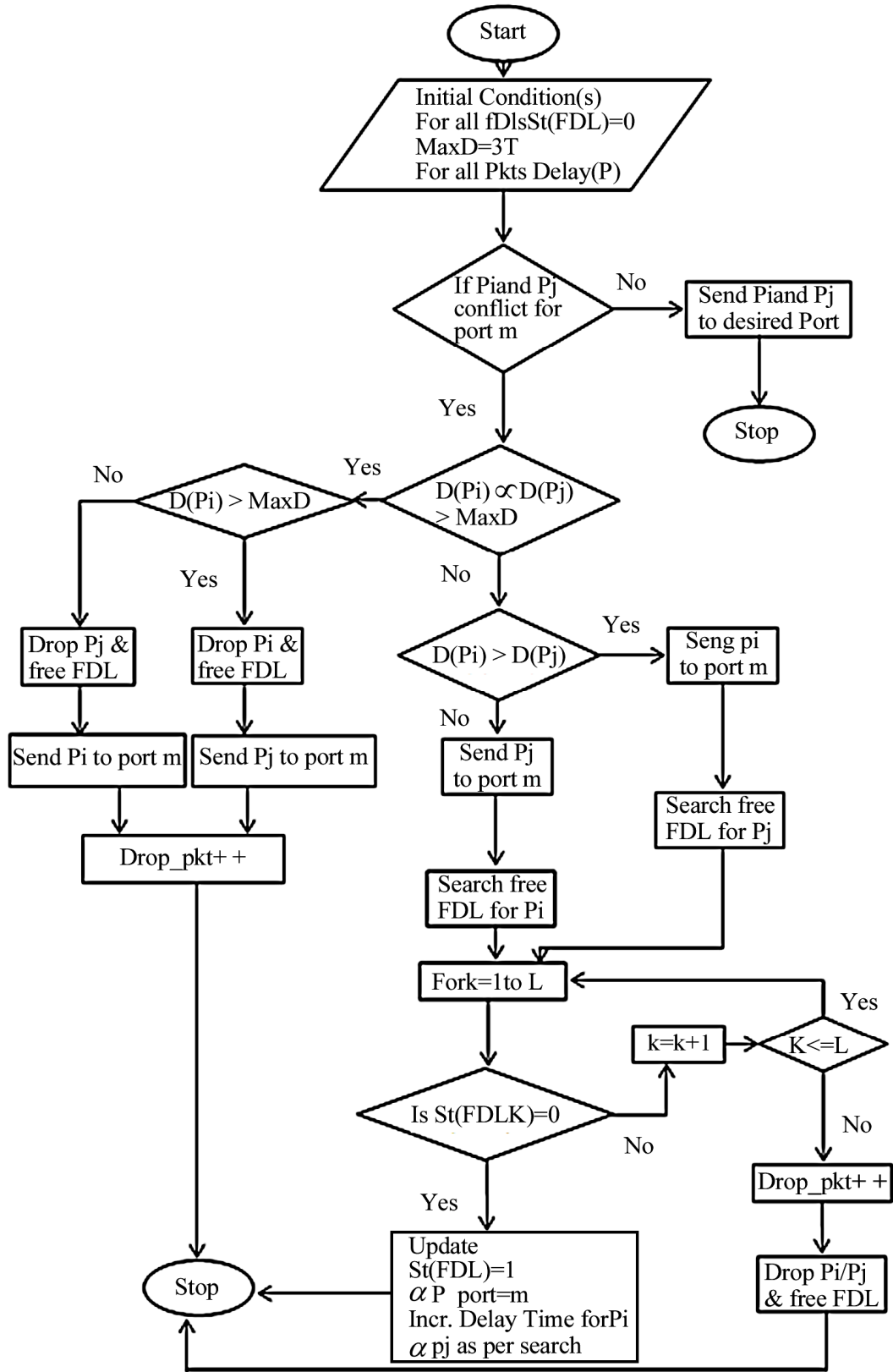


Figure 2. Flow Chart for the Contention Resolution Algorithm.

$$\rho = \frac{S\tau}{W(\sigma + \tau)} \quad (1)$$

A switch with M inputs and N outputs can be modeled as an M/M/N/N queue. The probability that the packet has to wait for service (i.e. packet blocking probability) is given by the following Erlang C formula

$$P(d > 0) = \frac{W\rho^w / W!(W-\rho)}{\sum_{i=0}^{w-1} \frac{\rho^i}{i!} + \frac{W\rho^w}{W!(W-\rho)}} \quad (2)$$

In the proposed switch architecture, if the destined output port for the packet is not free, it can be sent to one of the free FDL for a fixed amount of delay (i.e. equal to the packet transmission time). Assuming that total delay lines are D, becomes $L = W + D$ outputs. So now this can be modeled as M/M/L/L queue. The new packet delay probability can be given by following equation:

$$P'(d > 0) = \frac{\rho^L L / L!(L-\rho)}{\sum_{i=0}^{L-1} \frac{\rho^i}{i!} + \frac{\rho^L L}{L!(L-\rho)}} \quad (3)$$

Now the probability of number of packets delayed by more than t seconds can be calculated by multiplying the probability of number of packets delayed by time $t=0$ seconds with the negative exponential of $t\mu(L-\rho)$.

$$P(d > t) = P'(d > 0) \times e^{-t\mu(L-\rho)} \quad (4)$$

By using Equation (4) we can calculate the packet blocking probability for a given amount of delay time t seconds. For example for $t=1\text{ms}$ gives us the probability of number of packets that will be delayed by more than 1ms.

Here:

MaxD = Maximum delay for the packet

St(FDLk) = Status of FDLk (0 for free and 1 for busy)

D(Pi) = Delay for i^{th} packet

Drop_pkt = Drop packet count

3. Performance Evaluation and Discussion

The proposed switch architecture has been characterized for its packet delay performance and blocking probability under the influence of varying numbers of fiber delay lines. The performance of the proposed switch architecture handling eight channels has been evaluated and compared with conventional switch architecture.

The packet delay for the switch comprising of different number of delay lines in the switch is computed using Equation 4 and the corresponding results for delay lines having 1 to 4 are presented in Figure 3. It is observed that packet delay probability decreases with the inclusion

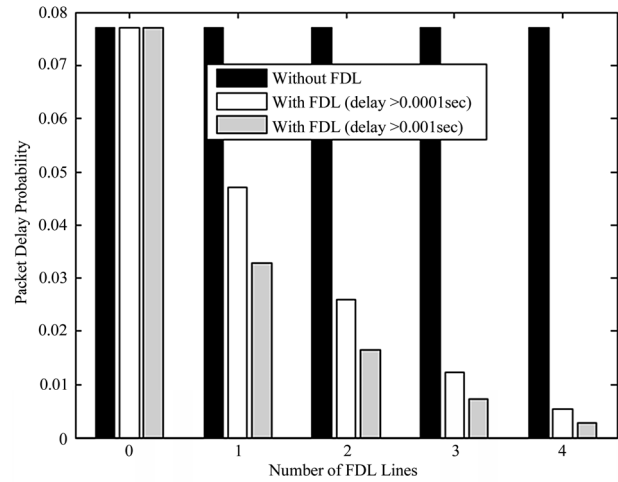


Figure 3. Packet delay probability for FDLs as a function of delay time with $\rho=5$ Erlang.

of more FDL lines. It is also inferred that the probability deteriorates for a given FDL structure by increasing packet delay time i.e. number of circulation allowed in FDLs. It depicts that the effect of increasing the number of FDLs on packet delay probability is more than increasing 10 times delay.

The influence of traffic load on the delay probability of the proposed switch architecture has been computed using the developed mathematical model and the results are depicted in Figure 4 for the case of delay time to packet hold time ratio as 1. It is observed that the delay probability is not a linear function of traffic intensity and increases rapidly with the rise in traffic at the lower traffic range however this dynamic gradient reduces at the higher traffic range in case of a normal switch without FDLs. In case of proposed switch architecture with a single FDL, the qualitative behavior of the delay probability is found to be similar but with a quantitative difference with a lower numerical value. It is further observed that inclusion of more FDLs in the switch makes the delay probability still lower values but not with a significant difference. It is interesting to note that though the numerical delay for a given load is lower for the FDLs in the switch, yet the gradient of the delay is slightly higher. This behavior reveals that in case of FDLs the traffic fluctuation may cause more variation in the delay probability as compared to a switch without FDLs. The packet delay analysis for different time delay to packet hold time ratio is obvious to appreciate physical operation of the switch. Figure 5 shows the variation of packet delay probability for the case of delay time to packet hold time ratio as 10. As we increase the delay time the delay probability decreases significantly due to more circulation in the delay lines finding a better probability of the packet to be processed. The curves in Figure 5 are qualitatively similar to the curves in the Figure 4 but

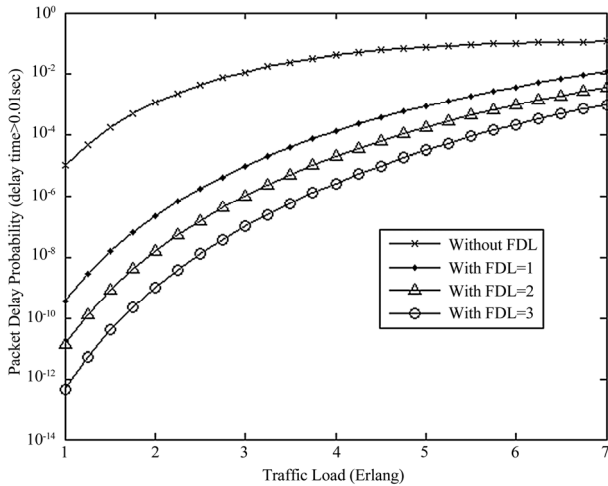


Figure 4. Packet delay probability as a function of the traffic load (ρ) for fixed size FDLs.

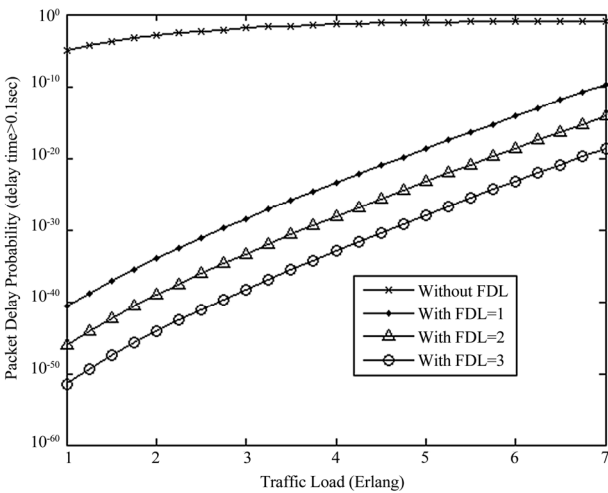


Figure 5. Packet delay probability as a function of the traffic load (ρ) for fixed size FDLs.

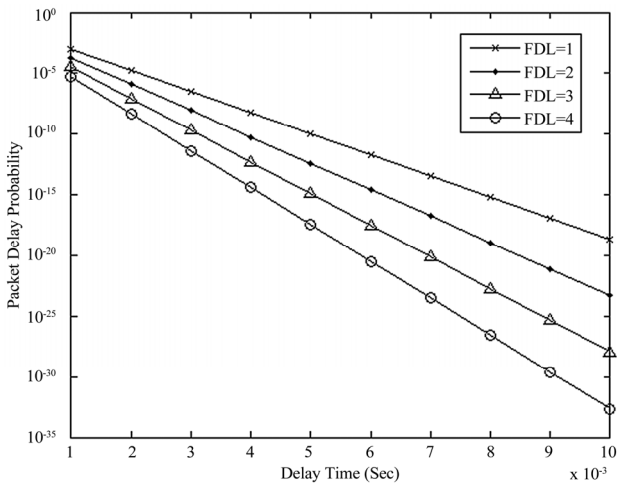


Figure 6. Packet delay probability as a function of the delay time for FDLs.

with a more significant numerical difference. The effect of delay time on packet delay probability with different number of FDLs has also been investigated and the results are shown in Figure 6. The packet delay probability decreases with the rise in the time delay in the switch and this tendency is maintained by further inclusion of FDLs in the switch. It may however be noted that slope of the curve is higher in case of the switch having more FDLs showing a better reduction in the packet delay probability with a slight increment in delay time.

4. Simulation Study

The proposed switch architecture has been simulated having 5 output ports with the varying number of FDLs from 1 to 4. The request set of varying size from one to ten units is randomly generated and is repeated 10 times for each random value. The number of circulation for each packet is varied from 0 to 3 for the simulation study and the results are presented in Figure 7. It is inferred that the throughput is almost equal for lower traffic (i.e. 10 to 30 requests) for different number of delay lines in the switch. This may be attributed to easy availability of the output ports for the lower incoming packet rate. However at moderate traffic rate (i.e. 40 to 70 requests) the availability of free output ports decreases due to packet contentions and thereby reduces the throughput for a less number of FDLs in the switch. The simulation curves also support the expected results showing a remarkable dropout in the throughput for the case of one FDL as compared with the four FDLs. It is also observed from the curves that the throughput difference decreases for higher traffic rate (i.e. 80 to 100 requests) and shows nearly the same throughput irrespective of the number of the FDLs showing the limiting packet handling capacity of the FDLs. It is observed that the FDLs are beneficial up-to certain traffic rate after that switch performance is controlled by input-output ports involved.

The switch behavior for the incoming traffic involving a three delay lines with different number of packet circulations in the FDLs has also been investigated. The simulation results have been presented in Figure 8 for the case of 0, 1, 2 and 3 circulation loops for the packets. It is obvious to note that no packet circulation loop shows the minimum throughput as compared to other cases. These curves also show that the throughput is improved significantly in case of circulating packets even for the single circulating loop for a moderate traffic rate. However these improvements are insignificant at lower and higher data rates due to constraints of the number of input-output ports.

The presented analysis confirms that switch size i.e. number of input-output ports, limits the throughput and makes it nearly constant after a given traffic rate. However

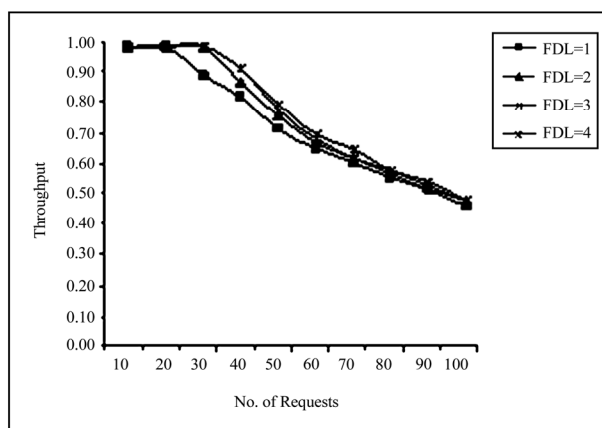


Figure 7. Throughput as a function of no. of requests for FDLs.

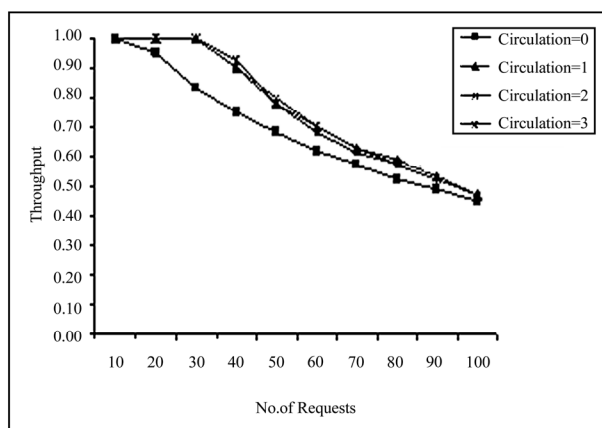


Figure 8. Throughput as a function of no. of requests for packet circulation(s).

this traffic limit is increased by using additional delay lines in the switch. This switch handling capacity may further improved by circulating the packets in delay lines providing the higher probability for finding the desired port at the output. Number of circulation is a notion of packet delay time and can be limited by the maximum time delay allowed in the switch.

5. Conclusions

A fiber delay line as a solution of packet contention in OPS network has been discussed to establish novel switch architecture with an appropriate mathematical model to simulate the traffic behavior. Model gives a more generic solution for the packet conflict problem at the switching node using FDLs. Packet circulation in delay lines is the key feature of the proposed method that improves connection probability up to a significant traffic rate. It also gives better utilization of FDLs through

packet circulation. Both theoretical and simulated results confirm each other. An important observation has been made out that the maximum number of FDLs and the circulations have a significant impact on throughput for a given switch. Performance analysis of the proposed switch architecture for asynchronous packet switching can be done as future work. Further this model can be analyzed with priority based packet scheduling algorithm to control the traffic.

6. References

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