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# Flipped Voltage Follower Ddesign Technique for Maximised Linear Operation

**Ching-Mei Chen, Khaled Hayatleh, Bryan Hart, John Lidgey**
*School of Technology, Oxford Brookes University, Oxford, UK*
*E-mail*: *khayatleh@brookes.ac.uk*
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## Abstract

The results of comparative DC simulation tests confirm that a proposed modification to the feedback circuit of a Flipped Voltage Follower (FVF), to produce a type of 'Folded' Flipped Voltage Follower (FFVF), is capable of maximising the linear DC operating range for given values of supply rail voltage and operating current.

**Keywords:** Analog, Voltage Follower

## 1. Introduction

The name 'Flipped Voltage Follower' (FVF) was coined by Carvajal *et al.* [1] to describe a class of pre-existing, and new, low power/low voltage analogue circuits.

A prototype FVF is a two transistor source-follower in which the input mosfet is forced to operate at a sensibly constant DC drain current, set by ancillary circuitry, despite variation in input voltage or load current. This is achieved by the action of shunt negative feedback.

The overall result is a source-follower with decreased output impedance and increased linearity in its voltage transfer characteristic. The so-called 'Super Source-Follower' [2] can be regarded as a member of the FVF family: in fact, it has been called a Folded Flipped Voltage Follower (FFVF) [3].

In **Figure 1**, M1 and M2 are inter-connected to form an N-channel FVF the operating current for which in supplied by $M_X$, the output mosfet of a simple 1:1 current mirror formed from $M_W$ and $M_X$. The mirror input current, $I_X$, is set by choice of $R_B$.

A capacitor, $C_S$ [1], may be required to produce a specified phase margin in the loop-gain frequency response.

M1 passes an effectively constant current so the incremental voltage gain of the FVF is close to unity providing it operates in its linear region. Unfortunately, as has been noted in [1], the valid linear range decreases with threshold voltage. This is most easily seen by applying Equations (1) and (2), which follow to the case in which the characteristics of M1 and M2 are identical.

From [4],

$$I_D = \frac{\beta_N}{2}\left(V_{GS} - V_{TN}\right)^2 \quad (1)$$

and, $$V_{DS(min)} = \sqrt{\frac{2I_D}{\beta_N}} \quad (2)$$

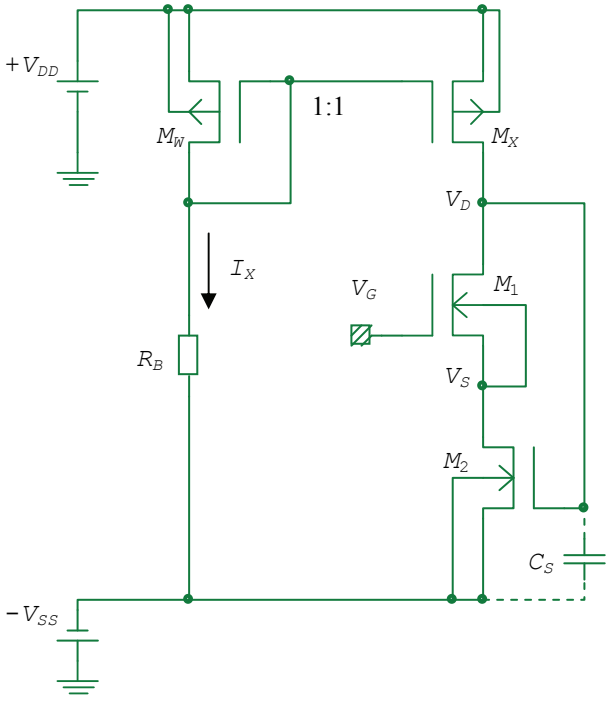


**Figure 1. A prototype Flipped Voltage Follower (FVF).**

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In these equations the symbols have their usual mosfet meanings:

$I_D$ = Drain Current; $V_{GS}(V_G\text{-}V_S)$ = Gate-source voltage; $V_{DS}(V_D\text{-}V_S)$ = Drain-source voltage; $V_{TN}$ = Threshold voltage; $\beta_N = \mu_N C_{OX}(W/L)$.

Linear operation requires both M1 and M2 to operate in the saturation region. Using Equations (1) and (2) the conditions for this for the circuit of **Figure 1** are,

$$V_G \geq -V_{SS} + 2\sqrt{\frac{2I_X}{\beta_N}} + V_{TN} \tag{3}$$

$$\text{and, } V_G \leq -V_{SS} + \sqrt{\frac{2I_X}{\beta_N}} + 2V_{TN} \tag{4}$$

If $\Delta V_G$ denotes the linear range then, from (3), (4),

$$\Delta V_G = V_{TN} - \sqrt{\frac{2I_X}{\beta_N}} \tag{5}$$

The problem, now, is that $\Delta V_G$ may be unacceptably small for the devices of modern CMOS technology, at even low values of $I_X$.

This problem does not arise in the new Folded Flipped Voltage Follower design technique described here because Equations (4) and (5) no longer apply.

For space reasons, the DC operating mode, only, is outlined here: small-signal performance is the subject of a future publication.

## 2. Proposed Circuit

**Figure 2** shows the proposed FFVF circuit. It differs from that of **Figure 1** (and that of [3]), by the way in which the feedback connection is made from the drain of M1 to the gate of M2. Instead of the direct link of **Figure 1** an additional mosfet, M3, is included and forced to operate at a sensibly constant current, $I_Z$, provided by the high output resistance Widlar-type current mirror formed from $M_Y$, $M_Z$ and $R_Z$. $M_X$ performs the same function as **Figure 1** but, in this case its output current is $I_Y$ so in normal operation the current in M1 is $(I_Y\text{-}I_Z)$.

M3 performs two functions. The first is to provide a feedback current, which is converted to a feedback voltage at the gate of M2. The second function of M3 is to keep the drain source voltage of M1 constant, preferably at the minimum level for saturation, with variation in $V_G$.

Using Equations (1) and (2), that can be achieved if,

$$\sqrt{\frac{2I_Z}{\beta_P}} + |V_{TP}| \geq \sqrt{\frac{2(I_Y - I_Z)}{\beta_N}} \tag{6}$$

in which subscript $P$ refers to $P$-channel mosfet M3.

A design requirement for the maximum linear range for $V_D$, and hence $V_S$, is for the equality sign in Equation (6) to hold under worst case operating conditions, *i.e.*, $I_Y$ and $\beta_P$ 'high' but $I_Z$, I$V_{TP}$I and $\beta_N$ 'low'.

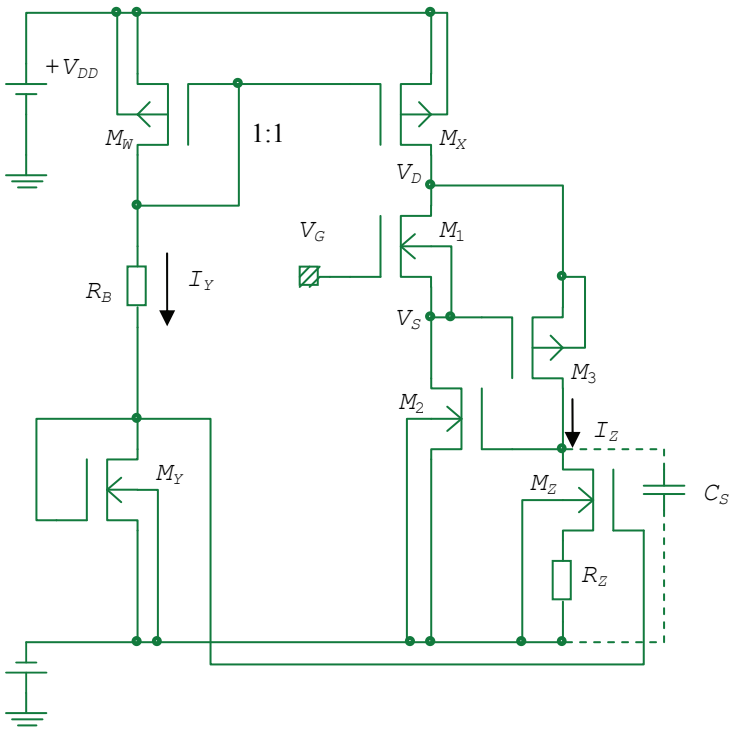


**Figure 2. Proposed circuit: A 'Folded' Flipped Voltage Follower (FFVF).**

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The upper limit to the linear range is governed by the onset of triode region operation in $M_X$.

Thus,

$$V_{S(max)} = V_{DD} - \sqrt{\frac{2(I_Y - I_Z)}{\beta_N}} - \sqrt{\frac{2I_Y}{\beta_P}} \qquad (7)$$

From a DC standpoint the choice of the ratio $I_Z/I_Y$ is not critical provided Equation (6) is satisfied. However, from a small signal viewpoint the choice of $I_Z$ affects the loop-gain characteristics via its effect on the dynamic parameters of M3.

## 3. Results

The circuits of **Figure 1** and **Figure 2** were simulated for operation at 27ºC. All the mosfets, except M3, had L = 0.13 u, W = 10 u. It was assumed that for low voltage/low power operation $V_{DD}$ and $V_{SS}$ would not exceed 1.5 V and $I_X$ would not exceed 1 mA, so these values were used in tests. For a fair comparison, M1 was made to operate at the same current in both circuits. For M3, the choices $I_Z$= 50 uA (so $I_Y$= 1.05 mA), L = 0.13 u, W = 50 u satisfied Equation (6).

Simulated test results, displayed for comparison, in **Figure 3**, **Figure 4** refer, respectively, to the circuits of **Figure 1** and **Figure 2**.

When $V_G$ is such that M1 is passing only a small leakage current the curves for $V_D$ in **Figures 3** and **4** are similar, as are those for $V_S$.

However, once M1 commences conduction differences appear. In **Figure 3** there is no region for which the voltage trace for $V_S$ is parallel to that for $V_G$ as would be the case for M1, M2 both operating in their saturated regions.

In **Figure 4** there is an extended region, above $V_G \cong$ 0.5 V where the voltage traces for $V_D$ (< $V_G$) and $V_S$ are parallel to that of $V_G$, in accordance with the theory presented. (Above $V_G$ = 1 V the onset of triode behavior in $M_X$ causes non linearity)

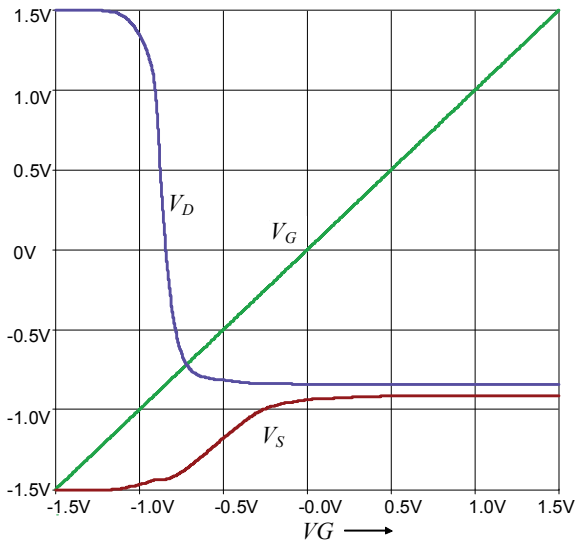


**Figure 3. Voltage traces for Figure 1 (See text for circuit details).**

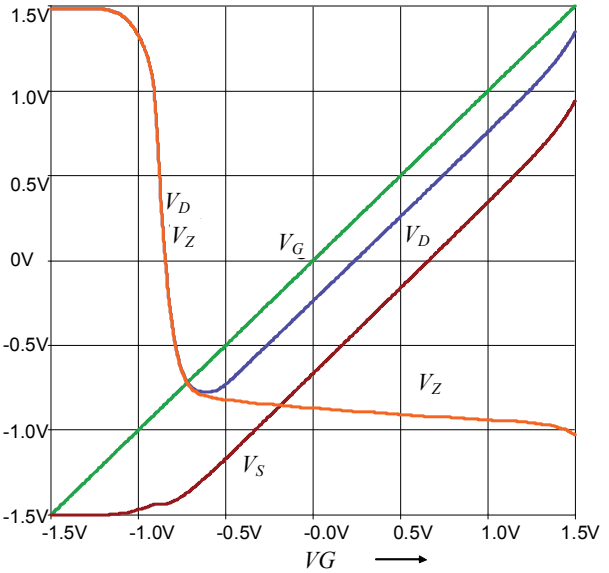


**Figure 4. Voltage traces for Figure 2 (See text for circuit details).**

## 4. Conclusion

The superior DC performance of the proposed FFVF, compared with that of the FVF is clearly evident.

## 5. References


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