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A 0.4 V Bulk-Driven Amplifier for Low-Power Data Converter Applications

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ABSTRACT

This paper presents the design of an ultra low-voltage (ULV) pseudo operational transconductance amplifier (P-OTA) that is able to operate with a single supply voltage as low as 0.4 V. The proposed circuit is based on the bulk-driven technique and use of cross-coupled self-cascode pairs that boosts the differential DC gain. The stability condition of this structure for the DC gain is considered by definition of two coefficients to cancel out a controllable percentage of the denominator. This expression for stability condition yield optimized value for the DC gain. Also, as the principle of operation of the proposed technique relies on matching conditions, Monte Carlo analyzes are considered to study of the behavior of the proposed circuit against mismatches. The designed P-OTA have a DC gain of 64 dB, 212 KHz unity gain bandwidth, 57˚ phase margin that is loaded by 10 pF differential capacitive loads, while consume only 16 μW. Eventually, from the proposed P-OTA, a low-power Sample and Hold (S/H) circuit with sampling frequency of 10 KS/s has been designed and simulated. The correct functionality for this configuration is verified from –30˚C to 70˚C. The simulated data presented is obtained using the HSPICE Environment and is valid for the 90 nm triple-well CMOS process.

Keywords: Pseudo Operational Transconductance Amplifier (P-OTA); Bulk-Input; Ultra Low-Voltage (ULV); Sample and Hold (S/H) Circuit

1. Introduction

The ultra low-voltage (ULV) supplies available in modern CMOS processes are a challenging matter for analog designers, and operation of ULV analog circuits has become inevitable due to scaling down of semiconductor technology [1-3]. This is evident from the International Technology Roadmap for Semiconductors (ITRS) [4]. This requires traditional circuit solutions to be replaced by new approaches to circuit design and more flexible structure strategies that are compatible with future standard CMOS technology trends. This is especially true for very high integration levels and very large scale integrated (VLSI) mixed-signal chips and SOCs. In mixed-signal systems, the analog circuits are combined with digital circuits in order to get the best performance with a low-voltage supply and low-power consumption. This combination should be done in an optimal way and the optimization process is application dependent. Recently, it has been possible to design circuits using power supplies as low as 1 V, and fabricated in the CMOS 90 nm technology. So far, CMOS 22 nm technology products will be available in the year 2013 with a power supply of 0.5 V [1]. While the supply voltage applicable in deep sub-submicron design will continue to decrease and eventually fall below 1 V, the threshold voltage will remain relative stable close to 250 mV [5-7]. This problem is mangified due to the fact that the threshold voltage (V_{th}) never decreases linearly with decreases in the power supply. There are a number of techniques for ultra low-voltage circuits such as use of self-cascode MOSFETs and cross-coupled pairs were proposed [1,2,8]. Meanwhile, self-cascode configuration connects the gates of two transistors together and provides high impedance with larger voltage headroom than the conventional cascode structure. The output resistance is roughly proportional to the transistors' dimensions and the effective voltage is the same as in a single MOSFET. Also, the bulk-input technique [9-14] shows a superior performance, which allows for operation in the moderate inversion region at supply voltages equal to the V_{th} of the technology. This technique, which uses the bulk terminal as signal input, is a promising method as it achieves enhanced performance without having to modify the exist-

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ing structure of the MOSFET [9-15]. Furthermore, the bulk-driven technique has better linearity and smaller power supply requirements. For a traditional MOSFET, the voltage applied to the bulk actually reduces the threshold voltage of the transistor, which increases the inversion level [16,17]. When applying this technique in circuit design, satisfactory performance can be achieved especially in ULV and low-power applications. OTAs are the key active building blocks of analog circuits. Fully differential OTAs are preferred because they provide larger signal swing, better distortion performance, better CM noise and supply noise rejection, but a CM feedback (CMFB) circuit must be added [18]. Also, fully differential OTAs work very well and can substantially improve the system's quality, especially in very unfriendly environments such as mixed-mode applications. However, at lower supply voltages, Pseudo OTAs (P-OTAs) could be used to avoid the voltage drop across the tail current source used in the fully differential structures. Various designs have been reported in the literature [1,8,16]. This paper presents the design of an ULV bulk-driven P-OTA in 90 nm triple-well CMOS technology with supply voltage as low as 0.4 V. As the principle of operation of the proposed technique relies on matching conditions, Monte Carlo analysis and Process-Voltage-Temperature (PVT) tests are considered to study of the behavior of the proposed circuit against mismatches. Eventually, from the proposed P-OTA, a low-power Sample and Hold (S/H) circuit has been designed and simulated. The design procedures of this structure are organized as follows. Sections 2.1 and 2.2 presents and analyses the small signal of the main P-OTA. In Sections 2.3 and 2.4 the bias circuit and CMFB structure are reviewed. Then S/H circuit is introduced in Section 2.5. Section 3 presents simulation results. Finally, the conclusion is given in Section 4. The Appendix gives details of the analysis.

2. Bulk-Input OTA Circuit Design

2.1. Main Amplifier Circuit

A very low-voltage bulk-input P-OTA without bias and CMFB circuits is shown in **Figure 1(a)**. Also, for small signal analysis, the AC model of this configuration is depicted in **Figure 1(b)**. In this structure, a PMOS P-OTA is implemented due to the action of M_{1x}, M_{2x}, M_{3x} and M_{4x}. The two inputs are on the bodies of PMOS transistors M_{1x} and M_{2x} and the body transconductance of these devices provides the input transconductance. These devices are loaded by the NMOS transistors M_{3x} and M_{4x}, which act as current sources. To further improve the differential gain, PMOS devices (M_{5x}, M_{6x} and M_{7x}, M_{8x}) are added. This configuration is a cross-coupled cascode pair that adds a negative resistance to the output and boosts the differential DC gain [19]. In this structure, the gate inputs of transistors M_{5x} and M_{6x} are biased at zero due to the limitation of the power supply voltage. Also, the gate inputs of M_{7x} and M_{8x} are connected to the gates of input transistors M_{1x} and M_{2x} and biased at 100 mV, which biases them in moderate inversion. Forward biasing of the body-source junction has been applied in low-voltage digital circuits [20-23] and it is applied here to lower the V_{th} of the transistors. We typically apply a forward bias up to 400 mV of V_{DD}, which results in a lowering of the V_{th} by about 50 mV. In the context of 0.4 V operation, the risk of forward biasing the junctions is minimized since parasitic bipolar devices cannot be activated even when the full power supply is used as forward bias. In addition, to obtain adequate gain, identical gain stages can be cascaded so that a two-stage P-OTA is obtained as shown in **Figure 1(c)**. In conclusion, the P-OTA is stabilized by adding Miller compensation capacitors C_c with series resistors R_c for right half-plane zero cancellation. In the designed P-OTA, C_c = 2.6 pF and R_c = 50 kΩ are assumed, respectively.

2.2. Small Signal Analysis

The drain-to-source accurrents of an NMOS and a PMOS transistor are given by

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + g_{ds} v_{ds} \tag{1}$$

$$i_{sd} = g_m v_{sg} + g_{mb} v_{sb} + g_{ds} v_{sd} \tag{2}$$

where *gm*, *gmb*, and *gds* are the gate transconductance, bulk transconductance, and output conductance, respectively. Then, using (1) and (2) and considering $v_{i-} = -v_{i+}$ and $v_{o-} = -v_{o+}$, we have

$$A_v = \frac{-g_{mb1}}{\left(g_{ds1} + g_{ds4} - \alpha \cdot g_{ds7}\right)} \tag{3}$$

$$\alpha = \frac{-\left(g_{mb5} - g_{ds5}\right)}{\left(g_{m5} + g_{mb5} + g_{ds5} + g_{ds7}\right)} \tag{4}$$

As can be seen from Equation (3) the conductance of $\alpha \cdot g_{ds7}$ can be used to boost the gain of the P-OTA. Identically, we define coefficients of $\beta\left(0 < \beta < 1\right)$ and g_{margin} due to process and temperature variations so that their $\alpha \cdot g_{ds7}$ term cancels out only β percent of the denominator. According to the above statement we can obtain the first stability conditions as follows:

$$\sum g_{\text{total}} = g_{ds1} + g_{ds3} - \alpha \cdot g_{ds7} > g_{\text{margin}} > 0 \tag{5}$$

$$g_{\text{margin}} = \beta \cdot \sum g_{\text{total}}, 0 < \beta < 1 \tag{6}$$

$$\sum g_{\text{total}} > \beta \cdot \sum g_{\text{total}} \Rightarrow \left(1 - \beta\right) \sum g_{\text{total}} > 0 \tag{7}$$

Then the maximum gain will be given by

$$A_{vMax} = \frac{-g_{mb1}}{\beta \cdot \sum g_{\text{total}}} = \frac{-g_{mb1}}{g_{\text{margin}}} \tag{8}$$

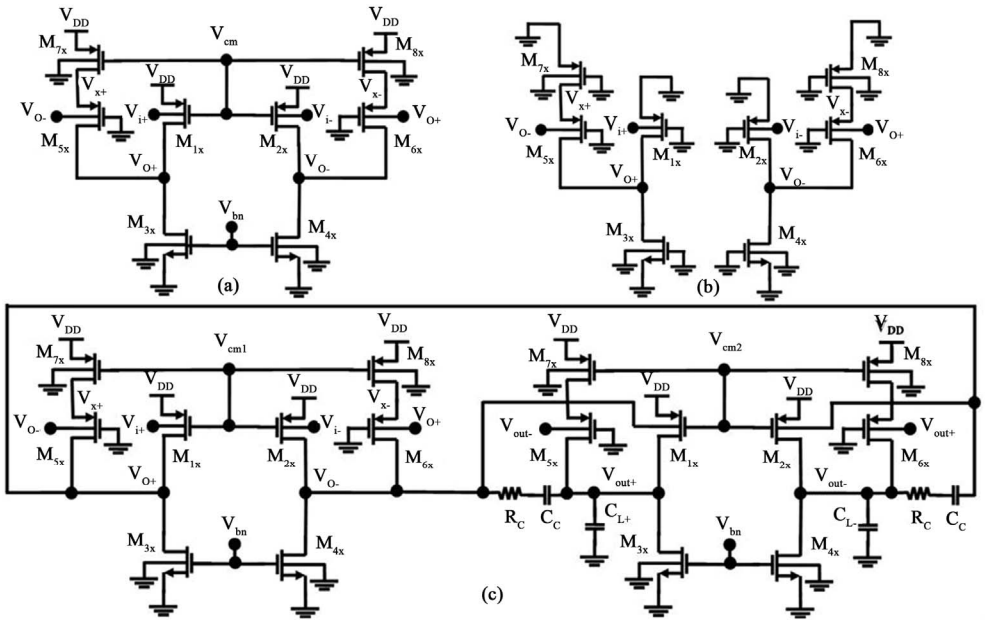

Figure 1. Proposed P-OTA: (a) One stage of the P-OTA; (b) AC model of the P-OTA; (c) Two-stage P-OTA with miller compensations.

We know that $0 < \beta < 1$; then

$$\sum g_{\text{total}} = g_{ds1} + g_{ds3} - \alpha \cdot g_{ds7} > 0 \tag{9}$$

$$g_{ds1} + g_{ds3} - \frac{\left(g_{mb5} - g_{ds5}\right)}{\left(g_{m5} + g_{mb5} + g_{ds5} + g_{ds7}\right)} \cdot g_{ds7} > 0 \tag{10}$$

We know that for boost, the gain must satisfy $\alpha < 0$. Therefore, the stability conditions for this structure can be expressed as:

$$\left\{ g_{ds1} + g_{ds3} > g_{mb5} > g_{ds5,7} \right\} \tag{11}$$

2.3. Common-Mode Feedback Circuit

Fully differential OTAs require a Common-Mode Feedback (CMFB) circuit. This circuit should behave linearly and only respond to CM voltage. A lack of this feature causes the Total Harmonic Distortion (THD) of the circuit to increase. Furthermore, a CMFB circuit amplifies the difference between the average of V_{o+} and V_{o-}, and sends a feedback signal V_{cm} to set the bias voltage at the gates of the input transistors of the OTA. Nowadays, designing a CMFB circuit which is able to operate under a ULV supply is very difficult, mainly because of the difficulty of detecting the CM voltage. In Reference [16] a CMFB circuit was designed which operated at 0.5 V by using two resistors to sense the output CM levels. But this structure increases the die area and reduces the gain due to larger loads on the OTA. To overcome some of these problems, a CMFB circuit has been reported [8] which is used in this paper and is depicted in **Figure 2**. The CM output voltage of first stage is not coupled to the CM output of the second stage. Therefore, two independent feedback circuits are needed to establish the CM voltage at outputs of the first and second stages. This structure uses four PMOS transistors, M_{c1} - M_{c4}, and two NMOS transistors, M_{c5} and M_{c6} in the first and second stages, respectively. The NMOS device is a bulk-input current mirror which compares the currents of the PMOS devices and then the difference between these currents is fed to the gate of the input transistors (V_{cm1} and V_{cm2}) to control the output CM voltages. This structure is able to operate with a ULV as low as 0.4 V.

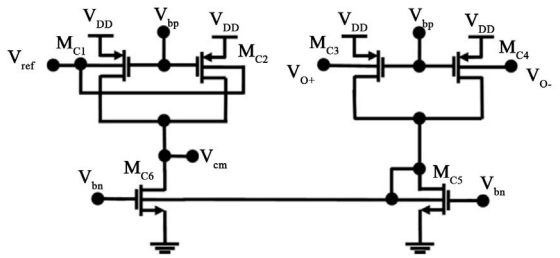

Figure 2. CMFB circuit used in reference [6] and proposed P-OTA.

2.4. Bias Circuit

A low-sensitivity reference current generator and bias circuit are illustrated in **Figure 3**. Due to limited voltage headroom, simple current mirrors are used to generate the bias voltages (V_{bn} and V_{bp}). Because the gate and source of M_{B3} and M_{B4} are common for both transistors, and the aspect ratios are equal, $I_{DM_{B3}} = I_{DM_{B4}}$.

Also, note that $V_{GSM_{B2}} = V_{GSM_{B1}} + R_B \cdot I_{DM_{B1}}$; thus

$$\sqrt{\frac{2I_{DM_{B3}}}{\mu_n \cdot C_{ox} \cdot (W/L)_{M_{B2}}}} = \sqrt{\frac{2I_{DM_{B3}}}{\mu_n \cdot C_{ox} \cdot K \cdot (W/L)_{M_{B2}}}} + R_B \cdot I_{DM_{B3}} \quad (12)$$

In the above mentioned equation, K is the ratio between the aspect ratios of M_{B1} and M_{B2}. Rearranging this expression,

$$I_{DM_{B3}} = \frac{1}{R_B^2} \frac{2}{\mu_n \cdot C_{ox} \cdot K \cdot (W/L)_{M_{B2}}} \left(1 - \frac{1}{K}\right)^2 \quad (13)$$

In the target circuit, K = 1.25 and R_B = 1 k, and thus a low sensitivity supply voltage independent reference current circuit is also designed and simulated which generates a stable 1 μA reference current for the bias circuit. As expected, the circuit is independent of the supply voltage. Transistor M_{B5} mirrors this current to generate a stable 1 μA reference current, which is used in the biasing of PMOS devices. In order to ensure that all the transistors operate in the saturation region, bias voltages V_{bn} and V_{bp} are applied to the gates of the NMOS and PMOS devices respectively in the P-OTA and CMFB circuits. These bias voltages have been tested versus temperature and power supply variations. For –30˚C to 70˚C temperature range and power supply variations of ±6.25%, the sensitivities of these voltages are about 0.24 mV/˚C and 0.33 mV/˚C, respectively.

2.5. Sample and Hold (S/H) Circuit

The in this section, the whole S/H circuit is introduced. The proposed structure has been implemented using CMOS 90 nm technology and simulated in Hspice Environment. **Figure 4** shows the entire S/H circuit. This circuit uses a two-phase, non-overlapping clock configuretion. Here, $\phi 1$ and $\phi 2$ are the non-overlapping clocks. The sampling frequency is 10 KS/s. During $\phi 1$ the input signal is sampled differentially, while during phase $\phi 2$ the P-OTA is put into a unity gain configuration.

For a power supply voltage of 0.4 V, and $V_{th} \approx 0.4$ V a transmission gate switch could possibly be used. However, the source of the switching transistor can be at a

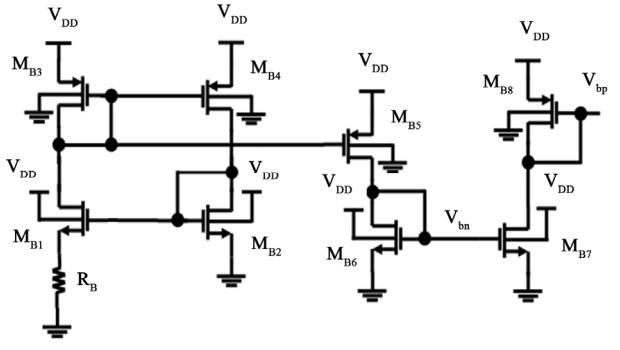

Figure 3. Reference current generator and bias circuit.

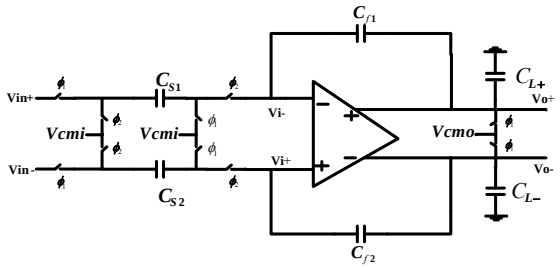

Figure 4. Sample and hold circuit.

very different voltage from the substrate, so the device threshold voltages can vary over the possible signal range [24] for typical process parameters. The well-known approach is use of Switched OTA circuits [25]. However, implementation of S/H using the switched OTA technique is impossible, while the circuits such as pipelined ADC converters require S/H operation at the input. Other approaches to overcome this problem are to use internal voltage boosting [26-32] that is used here. In voltage boosting techniques, some cases the clock voltage is doubled, and that can lead to reliability issues.

3. Simulation Results

Based on the analytical procedure described in the previous sections, a new ULV P-OTA was designed at a single supply voltage of 0.4 V from a 90 nm triple-well CMOS process and then simulated by HSPICE. The threshold voltages of this technology for NMOS and PMOS transistors are 0.42 V and –0.43 V, respectively. Then, from designed P-OTA, an ULV and low-power S/H circuit has been implemented.

3.1. Frequency and Transient Responses

The open-loop frequency response and closed-loop transient response of the P-OTA were tested. For a CM input of 200 mV, a DC gain of 64 dB, a bandwidth of 212 KHZ and a phase margin of 57˚ were obtained. **Figure 5** shows the frequency response of P-OTA. Also, to examine the effect of the doublet on the circuits' settling behaviors; the P-OTA was configured as closed-loop unity-gain amplifiers with 0.2 pF capacitors.

Then a 200 mV input CM voltage and a 100 mV step were applied to the P-OTA's input, and then output voltage with 1% error was observed. In this state, the output voltage settled to its final value in less than 4 μs for rising time and 3.3 μs for falling time, respectively. **Figure 6** shows the step responses of the P-OTA.

3.2. Monte Carlo Analyzes

Monte Carlo frequency and transient analyzes is considered to study of the behavior of the proposed circuit against mismatches. **Figures 7** and **8** show the Monte

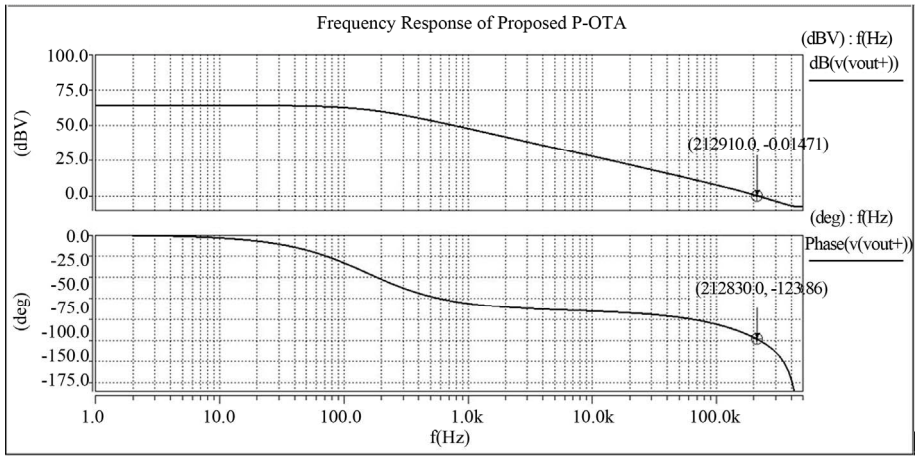

Figure 5. Frequency response of proposed P-OTA.

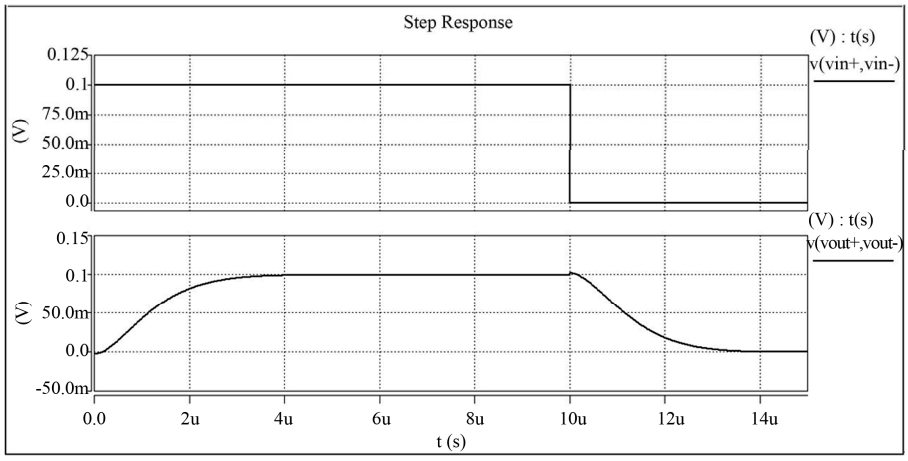

Figure 6. Settling simulated results of proposed P-OTA.

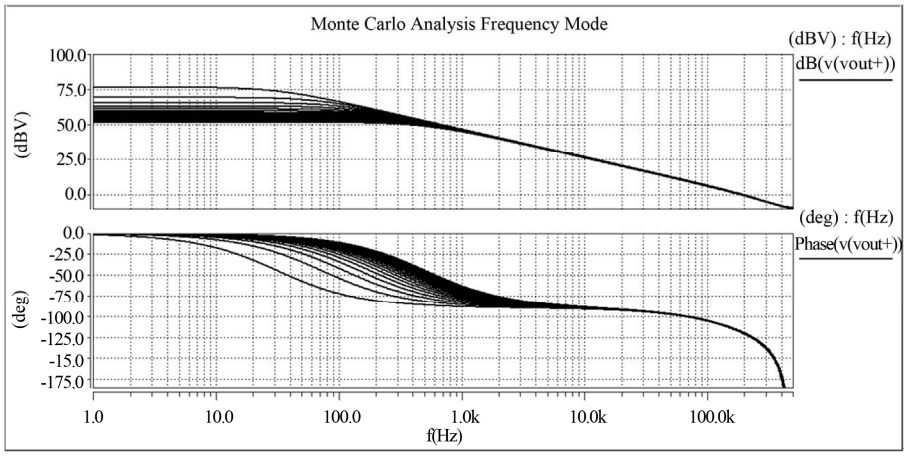

Figure 7. Monte carlo frequency analysis of proposed P-OTA.

Carlo analyzes of the P-OTA in frequency and transient modes. The result shows that the amplitude and the phase were almost independent of circuit parameters.

Also, in transient test the responses do not have any extra overshoot, because of the suitable bandwidth, phase margin and convenient CM output voltage. Also, this configuration was passed temperature variation from –30˚C to 70˚C.

3.3. Total Harmonic Distortion Response

The third obtained THD of the P-OTA, with a 200 mV amplitude and 500 Hz input frequency sampled at 10 KHz, were about 70 dB below the fundamental, as shown in **Figure 9**. It is obvious that the extra harmonics, but not the main harmonic have been eliminated. Finally, a comparison of proposed P-OTA with previous structures is summarized in **Table 1**.

3.4. Sample and Hold Output Responses

The input and output waveforms for a sinusoidal input of 200 mV peak-to-peak amplitude and 500 Hz frequency with a 10 KHz clock is depicted in **Figure 10**. To evaluate the nonlinearity, SNR and SNDR for mentioned input signal were also calculated. The result as indicated in **Figure 11** exhibits higher than 57.9 dB SNR and 56 dB SNDR that corresponds to 9 effective bits resolution. The

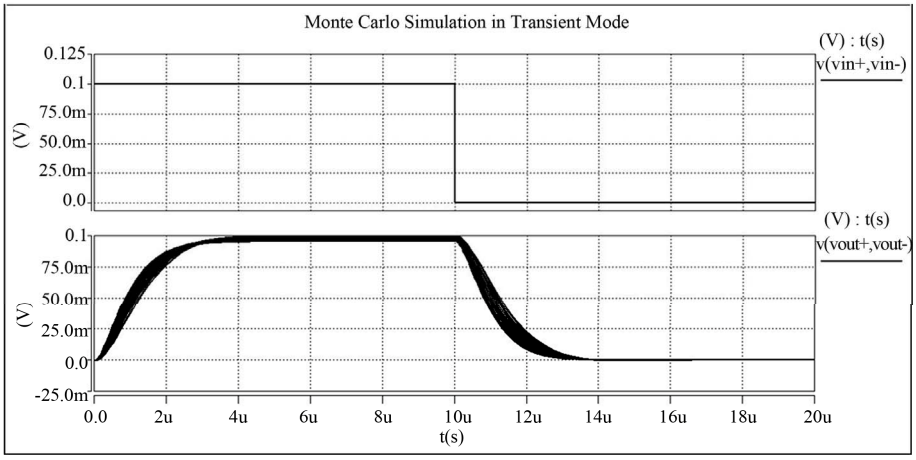

Figure 8. Monte carlo transient analysis of proposed P-OTA.

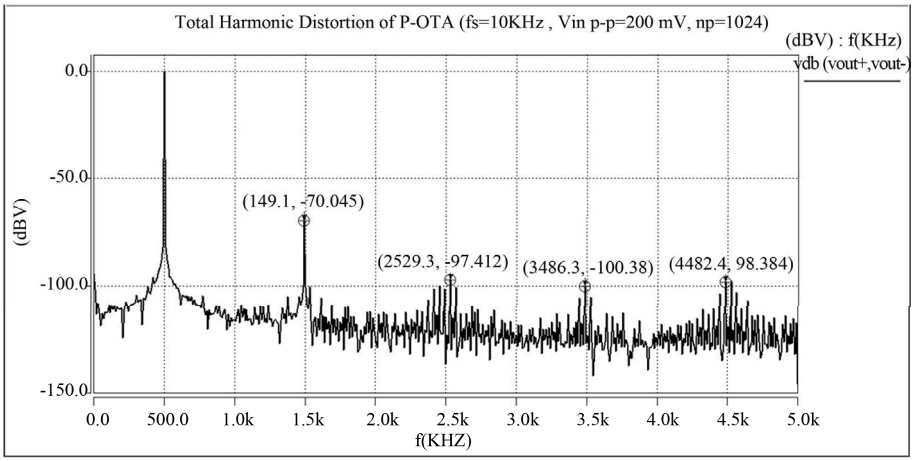

Figure 9. Total harmonic distortion of proposed P-OTA (Vinp-p = 200 mV, fin = 500 Hz, fs = 10 KS/s, n_p = 1024).

Table 1. Comparisons of characteristics of proposed P-OTAs with state-of-the-art P-OTAs.

Parameters	This work	[8]	[10]	[11]	[12]	[13]	[14]	[16]
Technology (nm)	90	180	350	350	350	350	180	180
Power supply (V)	0.4	0.5	1	1	0.6	1	0.9	0.5
DC gain (dB)	64	65	64	70.6	73.5	76.2	73.8	62
GBW (MHz)	0.212	0.55	2	4	0.01302	8.1	272	10
Phase-margin (˚)	57	50	45	65	54.1	63.14	64	60
THD (%)	0.31	0.13	NA	NA	0.13	NA	NA	1
Load capacitance (PF)	10	20	1	10	15	1MΩ‖17PF	2	20
Power dissipation (μW)	16	28	130	62	0.55	358	1420	*110*

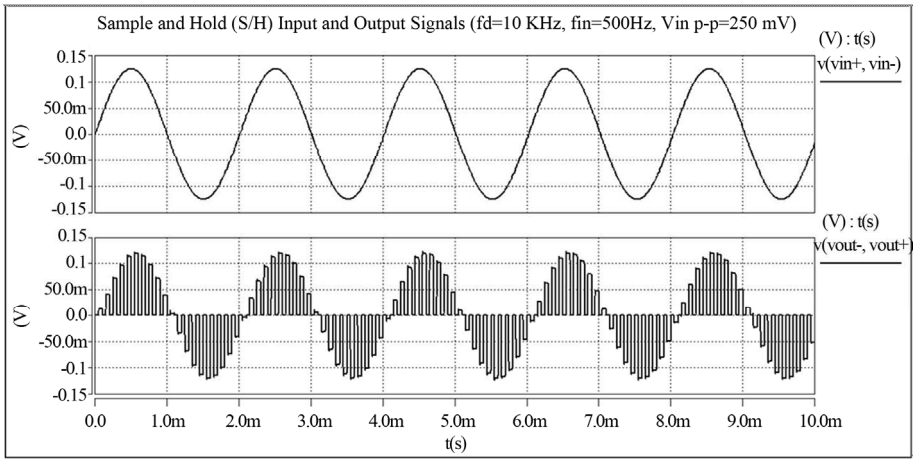

Figure 10. S/H input and output waves (fin = 500 Hz, fs = 10 KS/s).

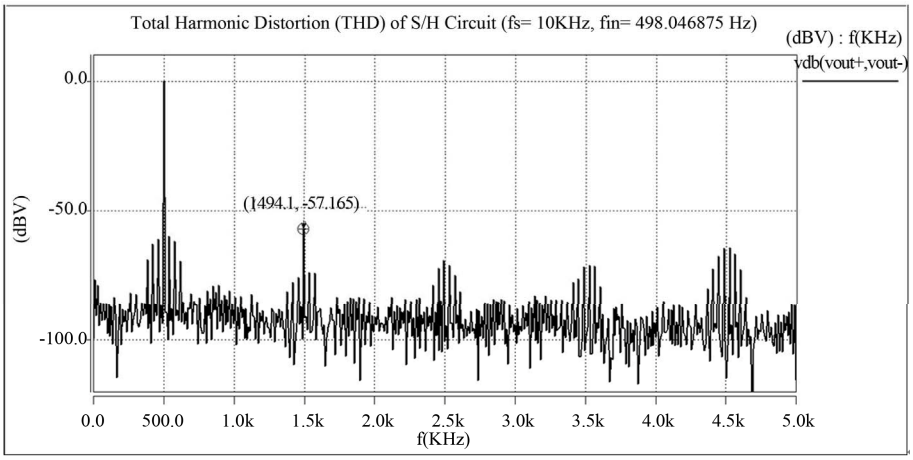

Figure 11. Total harmonic distortion of S/H (fin = 498.046875 Hz, fs = 10 KS/s, n_p = 1024).

Discrete Fourier Transform (DFT) of the data samples was also computed with the Hspice simulator. The result shows that the largest SPUR falls −57.16 dB below the RMS value of the fundamental corresponding to an SFDR of 57.16 dBc confirming the results obtained through nonlinearity evaluation.

4. Conclusion

A new bulk-driven pseudo OTA topology using of cross-coupled self-cascode pairs technique has been presented. The operation principle of proposed structure is based on modifying the effective conductance of the active loads and enhancing the effective transconductance. This structure has been simulated in the 90 nm triple-well CMOS process with a supply voltage as low as 0.4 V. The proposed cross-coupled self-cascode pairs add a negative resistance to the outputs of structure and boost the differential DC gain. Also, expression for the DC gain was given, which can be solved for the small signal analysis. Then, in this structure, the stability condition of the presented technique for the DC gain has been considered by definition of two coefficients to cancel out a controllable percentage of the denominator. This expression for stability condition yield optimized value for the DC gain. Besides, the exact expressions for the transfer function coefficients presented in the Appendix were verified for a number of different sets of component values. The transfer function coefficients were calculated using the formulas in the Appendix, the poles and zero(s) were found by factoring the numerator and denominator of the transfer function, and those results were compared to the poles and zero(s) from a HSPICE [33] pole-zero analysis of the same small-signal circuit. For future work, the optimized parameters can be found using a Genetic Algorithm (GA) to get a high performance structure in analog integrated circuits. The P-OTA provides a DC gain of 64 dB, a phase margin of 57˚ and an open loop unity-gain frequency of 212 KHz with a 10 pF capacitive load. The total current of the P-OTA is 40 μA. In this design, the first and second stages consume about (1/3) and (2/3) of the total power consumption. Also, an output swing of ±0.12 V was obtained for proposed structure.

Furthermore, THDs of −70 dB was given for 200 mV amplitude and 500 Hz input frequency sampled at 10 KHz. In spite of the ULV, excellent supply rejections of 71 dB at 5 KHz was obtained. Also, a reasonable CM rejection ratio of 81 dB at same frequency was achieved. However, the smaller bulk transconductance and large capacitance from the body to the substrate, limit the bandwidth of the structures. Eventually, from the proposed P-OTA, a low-power S/H circuit with sampling frequency of 10 KS/s has been designed and simulated. In addition, the preliminary simulation results demonstrate the feasibility of the P-OTA for modern ULV and low-power mixed-signal chips and SOCs.

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Appendix

In addition, the transfer function and pole zero (s) analysis of the small-signal circuit in **Figure 1(c)** is analyzed here. With appropriate substitutions, the results of this analysis can be used for other related circuits in analog integrated circuit design. According to Equations of the first and second stages that is neglected here, a circuit model was obtained, which is shown in **Figure A1**. We know that the poles in this structure can be real or complex, depending upon the element values.

However, real or complex non-dominant poles can occur in practice and can be calculated using the denominators' roots from Equations in (A.12), using the exact transfer function coefficients presented in this paper.

Transfer Function Calculation

Writing KCL at the nodes $V_{x1,2}$, V_{o+} and $V_{\text{out}-}$ for the first and second stages, yields

$$i_2' = -Y_2' \cdot v_{x2} = G_1' \cdot v_{x2} + G_2' \cdot v_{\text{out}-} \tag{A.1}$$

$$v_{x2} = \left[-G_2' / \left(G_1' + Y_2'\right)\right] \cdot v_{\text{out}-} = -\alpha' \cdot v_{\text{out}-} \tag{A.2}$$

$$\alpha' = \frac{G_2'}{\left(G_1' + Y_2'\right)} \tag{A.3}$$

$$i_1' = Y_1' \cdot v_{\text{out}-} \tag{A.4}$$

$$i_2' = i_1' + g_{mb2} \cdot v_{o+} + Y_c \left(v_{\text{out}-} - v_{o+}\right) \tag{A.5}$$

Substituting (A.1) and (A.4) in (A.5) result in

$$\frac{v_{\text{out}-}}{v_{o+}} = \frac{-\left(g_{mb2} - Y_c\right)}{\left[Y_1^{'} + Y_c - \dfrac{Y_2' \cdot G_2'}{\left(G_1' + Y_2'\right)}\right]} \tag{A.6}$$

In addition, for the first stage we have

$$i_2 = -Y_2 \cdot v_{x1} = G_1 \cdot v_{x1} + G_2 \cdot v_{o+} \tag{A.7}$$

$$v_{x1} = \frac{-G_2}{\left(G_1 + Y_2\right)} \cdot v_{o+} = -\alpha \cdot v_{o+} \tag{A.8}$$

$$\alpha = \frac{G_2}{\left(G_1 + Y_2\right)} \tag{A.9}$$

$$i_1 = Y_1 \cdot v_{o+} \tag{A.10}$$

$$i_2 = i_1 + g_{mb1} \cdot v_{i+} + Y_c \left(v_{o+} - v_{\text{out}-}\right) \tag{A.11}$$

Substituting (A.7) and (A.10) into (A.11) yields

$$A_v(s) = \frac{g_{mb1} \cdot \left(g_{mb2} - Y_c\right)}{\left[\left(Y_1 + Y_c - Y_{cs}\right)\left(Y_1' + Y_c - Y_{cs}'\right) + Y_c \cdot \left(g_{mb2} - Y_c\right)\right]} \tag{A.12}$$

Pole-Zero Analysis

In this Section, to perfect the design in the first and second stages of P-OTA and pole and zero(s) analysis, we assume that $\alpha = 0\left(g_{mb5} = g_{ds5}\right)$ and $\alpha' = 0\left(g_{mb6} = g_{ds6}\right)$. So, from Equation (A.12) we manipulate the desired P-OTA gain v_{out}/v_i. The gain transfer function is (see formula (A.13)),
assuming that

$$R_C = \frac{1}{g_{mb2}} \tag{A.14}$$

$$\tau_c \cdot \tau_{o1} = R_C C_C \cdot R_{o1} C_1 = \frac{R_C C_C C_1}{\left(g_{ds1} + g_{ds3}\right)} \ll 1 \tag{A.15}$$

$$\tau_c \cdot \tau_{o2} = R_C C_C \cdot R_{o2} C_1' = \frac{R_C C_C C_1'}{\left(g_{ds2} + g_{ds4}\right)} \ll 1 \tag{A.16}$$

the approximate gain transfer function will be as follows

$$A_v(s) = \frac{A_0 \cdot \left(1 + \tau_c \cdot S\right)}{\left[\left(1 + \tau_1 \cdot S\right)\left(1 + \tau_2 \cdot S\right) + \dfrac{C_C \cdot A_0 \cdot S}{g_{mb1}}\right]} \tag{A.17}$$

Rewriting (A.17), we obtain

$$A_v(s) = \frac{A_0 \cdot \left(1 + \tau_c \cdot S\right)}{\left[1 + \left(\tau_1 + \tau_2 + \dfrac{C_C \cdot A_0}{g_{mb1}}\right) \cdot S + \tau_1 \tau_2 \cdot S^2\right]} \tag{A.18}$$

Using (A.18), the poles and zero can be expressed as

$$z = \frac{-1}{\tau_c} = \frac{-1}{R_C \cdot C_C} \tag{A.19}$$

$$P_{1,2} = \frac{-\left(\tau_1 + \tau_2 + \dfrac{C_C \cdot A_0}{g_{mb1}}\right) \pm \sqrt{\left(\tau_1 + \tau_2 + \dfrac{C_C \cdot A_0}{g_{mb1}}\right)^2 - 4\tau_1 \tau_2}}{2} \tag{A.20}$$

Poles P_1 and P_2 will be real and widely spaced if

$$\left(\tau_1 + \tau_2 + \frac{C_C \cdot A_0}{g_{mb1}}\right)^2 \gg 4\tau_1 \tau_2 \tag{A.21}$$

Squaring both sides and rearranging yields

$$A_v(s) = \frac{A_0 \cdot \left(1 + \tau_c' \cdot S\right)\left(1 + \tau_c \cdot S\right)}{\left[\left(1 + \tau_1 \cdot S + \tau_c \tau_{o1} \cdot S^2\right)\left(1 + \tau_2 \cdot S + \tau_c \tau_{o2} \cdot S^2\right) + \dfrac{C_C \cdot A_0 \cdot S}{g_{mb1}}\left(1 + \tau_c' \cdot S\right)\right]} \tag{A.13}$$

$$\left(\sqrt{\tau_1}-\sqrt{\tau_2}\right)^2+\frac{C_C\cdot A_0}{g_{mb1}}\gg 0 \qquad \text{(A.22)}$$

Finally, the requirements of the exact expressions for the coefficients are summarized in **Table A1**.

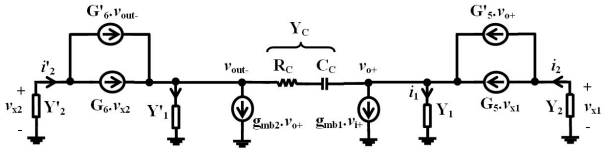

Figure A1. Circuit Model of the Proposed P-OTA.

Table A1. The exact expressions for the coefficients of the proposed P-OTA.

Parameters	Definition of parameters
Y_1	$g_{ds1}+g_{ds3}+S\cdot C_1$
Y_2	$g_{ds7}+S\cdot C_2$
C_1	$C_{db1}+C_{db3}+C_{db5}$
C_2	$C_{gs5}+C_{db7}$
Y_1'	$g_{ds2}+g_{ds4}+S\cdot C_1'$
Y_2'	$g_{ds8}+S\cdot C_2'$
C_1'	$C_{db2}+C_{db4}+C_{db6}+C_L$
C_2'	$C_{gs6}+C_{db8}$
$G_1=G_5=G_{6+}$	$G_1=G_{6+}=g_{m5}+g_{mb5}+g_{ds5}$
$G_2=G_5'=G_{5+}$	$G_2=G_5'=g_{mb5}-g_{ds5}$
$G_1'=G_6=G_{6-}$	$G_1'=G_6=g_{m6}+g_{mb6}+g_{ds6}$
$G_2'=G_6'=G_{5-}$	$G_2'=G_6'=g_{mb6}-g_{ds6}$
Y_c	$\left(R_C+1/S\cdot C_C\right)^{-1}$
α	$G_2/\left(G_1+Y_2\right)$
α'	$G_2'/\left(G_1'+Y_2'\right)$
Y_{cs}	$\alpha\cdot Y_2$
Y_{cs}'	$\alpha'\cdot Y_2'$
A_0	$g_{mb1}\cdot g_{mb2}/\left(g_{ds1}+g_{ds3}\right)\left(g_{ds1}+g_{ds3}\right)$
τ_c'	$\left(R_C-1/g_{mb2}\right)\cdot C_C$
τ_c	$R_C\cdot C_C$
τ_1	$\tau_c+\tau_{o1}+\tau_{c1}$
τ_{o1}	$R_{o1}\cdot C_1$
τ_{c1}	$R_{o1}\cdot C_C$
R_{o1}	$\left(g_{ds1}+g_{ds3}\right)^{-1}=r_{ds1}\left\|r_{ds3}\right.$
τ_2	$\tau_c+\tau_{o2}+\tau_{c2}$
τ_{o2}	$R_{o2}\cdot C_1'$
τ_{c2}	$R_{o2}\cdot C_C$
R_{o2}	$\left(g_{ds2}+g_{ds4}\right)^{-1}=r_{ds2}\left\|r_{ds4}\right.$

