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Versatile Voltage-Mode Universal Filter Using Differential Difference Current Conveyor

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Abstract

A novel four-input three-output voltage-mode differential difference current conveyor (DDCC) based universal filter is presented. The circuit uses three DDCCs as active elements, two resistors and two capacitors as passive elements. The circuit along with its versatility enjoys the advantage of minimum number of passive elements employment. SPICE simulation results are given to confirm the theoretical analysis. The proposed circuit is a novel addition to the existing knowledge on the subject.

Keywords: Analog Filters, Current Conveyors, DDCC, Voltage-Mode, Universal Filter

1. Introduction

Current-mode circuits have wider bandwidth, larger linearity, higher slew-rate, and wider dynamic range than voltage-mode circuits, thus they have received considerable attention [1]. A number of applications, such as filters, oscillators, analog-digital converter, and analogue signal processing blocks based on current conveyors have been proposed [2-4]. Recently, current-mode circuits are well used in communication circuits and wireless optical systems due to their larger dynamic range and wider bandwidth [5-6].

In 2004, Jianping Hu [7] proposed a CMOS DDCC along with its filtering applications. In the same year, Horng [8] proposed a similar a voltage mode multifunction filter with a single input and three outputs, which can realize low-pass, band-pass and high-pass filter functions by using two DDCCs, two grounded resistors and two grounded capacitors. But these configurations could not realize all-pass and band-stop functions. In 2004, Temizyurek [9] proposed a three-input single-output voltage mode universal filter. This configuration can realize low-pass, band-pass, band-stop, high-pass and all-pass filter functions using two DDCCs as active device and two resistors and two capacitors as passive devices, but there was no inverted output. In 2007, Chen [10] proposed a universal voltage mode single-input multiple output filter with two DDCCs, two grounded capacitors and three resistors. This configuration can give band-pass, band-stop, high-pass, all-pass and inverting low-pass responses. In 2007 again, Chen [11] proposed two single DDCC based configurations. These were single-input multiple output filters and could provide low-pass, band-pass and high-pass functions. In 2008, a compact voltage-mode multifunction filter employing only one DVCC and four components was reported [12]. Very recently, a single input three output universal filter using three DVCC/DDCC and only four components was also reported [13]. These works [12-13] were based on use of four passive elements and thus lacked non-interactive control of pole-frequency and quality factor. More recently, another biquad filter using DVCC was further proposed [14].

This paper presents a new Biquadratic filter configuration with three DDCCs, two resistors, and two capacitors. This configuration provides low-pass functions, band-pass functions, band-stop functions, high pass functions and all-pass functions, each with inverting and non-inverting transfer functions. The proposed circuit is verified through PSPICE simulations using 0.5 μm CMOS parameters with good results.

2. Differential Difference Current Conveyor

The DDCC, whose symbol is shown in **Figure 1** is a six port building block. The DDCC is characterized by the following equations:

$$I_{Y1} = I_{Y2} = I_{Y3} = 0 \quad (1)$$

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \quad (2)$$

$$I_{Z+} = I_X \quad (3)$$

$$I_{Z-} = -I_X \quad (4)$$

where, suffixes refer to the respective terminals.

The CMOS Differencial Difference Current Conveyor used in this work was introduced in 2004 [7]. The CMOS implementation of DDCC is shown in **Figure 2**.

The input transconductance elements are realized with two differential stages (M1 and M2, M3 and M4). The high gain stage composed of a current mirror (M7 and M8) which converts the differential current to a single ended output current. Transistors M9-M12 are used to reduce the current error due to different drain voltages of M7 and M8 between currents I7 and I8. The transistors M9 and M13 provide negative feedback to make voltage V_X less dependent of the current drawn from X-terminal. The small resistance R_X [7] can be expressed as

$$R_X = \frac{(g_{d1} + g_{d4} + g_{d8})(g_{d9} + g_{d12})}{g_{m4} g_{m9} g_{m13}} \quad (5)$$

Equation (5) simply gives a measure of intrinsic resistance at X terminal of DDCC. The current through terminal X is conveyed to Z+ terminal by the current mirrors formed by transistors M13, M15 and M14, M16. Similarly, M17-M22 performs current inversion so as to provide $Z-$ output [7].

3. Proposed Circuit

3.1. Circuit Description

The proposed circuit configuration is shown in **Figure 3**. The proposed circuit is a multiple input multiple output filter which can give various filter functions at its three outputs based on the combination of input terminals used. The circuit has one high input impedance terminal and three other input terminals and three output terminals. The circuit has three DDCCs, two grounded resistors and two capacitors.

The output transfer functions of **Figure 3** can be expressed as

$$V_{o1} = \frac{sC_2R_2v_{i1} + \left(s^2C_1C_2R_1R_2\right)v_{i2} - \left(sC_2R_2\right)v_{i3} + v_{i4}}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \quad (6)$$

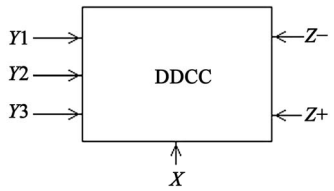

Figure 1. Symbol of DDCC.

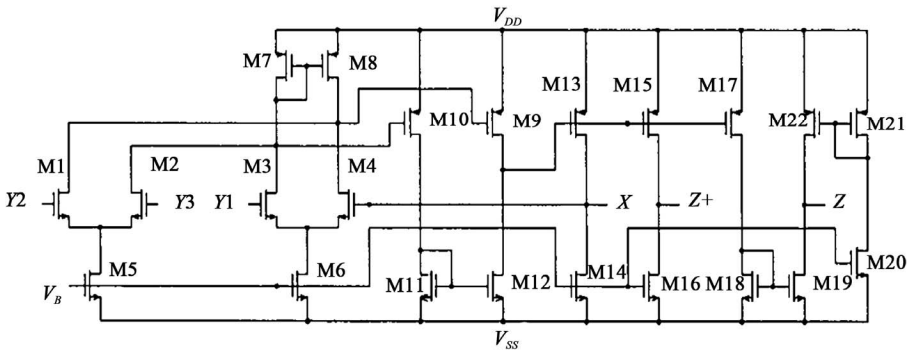

Figure 2. CMOS implementation of DDCC [7].

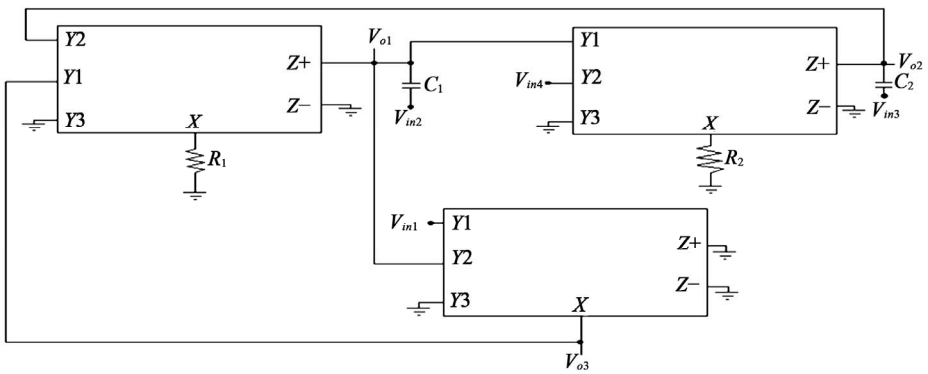

Figure 3. Proposed multi-input multi-output universal filter.

$$V_{o2} = \frac{v_{i1} + sC_1R_1v_{i2} + \left(s^2C_1C_2R_1R_2 + sC_2R_2\right)v_{i3} - \left(sC_1R_1 + 1\right)v_{i4}}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \quad (7)$$

$$V_{o3} = \frac{\left(s^2C_1C_2R_1R_2 + 1\right)v_{i1} - s^2C_1C_2R_1R_2v_{i2} + sC_2R_2v_{i3} - v_{i4}}{s^2C_1C_2R_1R_2 + sC_2R_2 + 1} \quad (8)$$

The ω_0 and Q of the filter is given by

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}} \quad Q = \sqrt{\frac{C_1R_1}{C_2R_2}} \quad (9)$$

The proposed configuration is capable of implementing as many as 8 filtering functions with suitable choice of inputs and outputs as depicted in **Table 1**. It may be noted that 'NI' refers to 'non-inverting', whereas 'I' refers to 'inverting'. V_{in} refers to the node's (input) connection to input signal.

3.2. Non-ideal Study

Taking the non-idealities of DDCCs in to account, the relationship of the terminal voltages and currents can be rewritten as

$$\begin{aligned} V_X &= \beta_{1k}V_{Y1} - \beta_{2k}V_{Y2} + \beta_{3k}V_{Y3} \\ I_{Y1} &= I_{Y2} = I_{Y3} = 0 \\ I_{Z+} &= \alpha_{1k}I_X \\ I_{Z-} &= -\alpha_{2k}I_X \end{aligned} \quad (10)$$

In Equation (10), β_{1k}, β_{2k}, and β_{3k} are respectively the voltage transfer gains from Y_1, Y_2 and Y_3 terminals to the X-terminal for the kth DDCC. Moreover, α_{1k} and α_{2k} are the current transfer gains for kth DDCC from X to Z+ and Z– terminals respectively. The non ideal analysis of the proposed circuit gives the characteristic equation as:

$$D(s) = s^2 + \alpha_1\beta_{11}\beta_{32}\left(s/C_1R_1\right) + \alpha_1\alpha_2\beta_{21}\beta_{12}/C_1C_2R_1R_2 \quad (11)$$

Therefore,

$$\omega_0 = \sqrt{\frac{\alpha_1\alpha_2\beta_{21}\beta_{12}}{C_1C_2R_1R_2}} \quad (12)$$

$$Q = \frac{\sqrt{\alpha_2\beta_{21}\beta_{12}/\alpha_1}}{\beta_{11}\beta_{32}}\sqrt{\frac{C_1R_1}{C_2R_2}} \quad (13)$$

Equations (12)-(13) show that the non-ideal transfer gains affect the filter parameters. The sensitivity of parameters to the same is found to be within unity in magnitude, thus showing good sensitivity performance.

4. Simulation Results

To verify the theoretical prediction of the proposed Biquadratic filter, PSPICE simulations were carried out for a designed frequency, f_0 = 1.0065 MHz and gain of all filters as 'unity': C_1 = 10 pF, C_2 = 25 pF, R_1 = 10 K, R_2 = 10 KΩ for few selected combinations. The supply voltages used was ±2.5 V.

Case-1: Low pass, band pass and band stop responses (choice No. 1)

If $V_{i1} = V_{in}$ (the input voltage signal) and $V_{i2} = V_{i3} = V_{i4} = 0$ (namely, the capacitor C_1 and C_2 are grounded), then the non-inverting band-pass (NI-BP), non-inverting low-pass (NI-LP) and non-inverting band-stop (NI-BS) filters are obtained at the node voltages, V_{o1}, V_{o2} and V_{o3}, respectively. Note that the input signal, $V_{i1} = V_{in}$, is connected to the high-input impedance input node of the DDCC (the Y_1 port of the DDCC). So the circuit enjoys the advantage of having high-input impedance, leading to cascadability at the input port.

Table 1. Choice of inputs and outputs to implement different filtering functions.

Choice No.	Input conditions				Outputs		
	V_{i1}	V_{i2}	V_{i3}	V_{i4}	V_{o1}	V_{o2}	V_{o3}
1.	V_{in}	0	0	0	NI-BP	NI-LP	NI-BS
2.	0	V_{in}	0	V_{in}	NI-BS	NI-LP	I-BS
3.	0	V_{in}	0	0	NI-HP	NI-BP	I-HP
4.	V_{in}	0	0	V_{in}	-	I-BP	NI-HP
5.	0	V_{in}	V_{in}	V_{in}	NI-AP	-	I-AP
6.	0	0	0	V_{in}	NI-LP	-	I-LP
7.	V_{in}	V_{in}	0	0	-	-	NI-LP
8.	0	0	V_{in}	0	I-BP	-	NI-BP

Figure 4 shows the filter response for low pass, band pass and band reject functions. The low pass band width found is 0.89615 MHz. Similarly for band pass function the central frequency is 1.042 MHz and the band width is 1.041 MHz. While for the band reject function the central frequency found is 1.0278 MHz. **Figure 5** shows the transient response of band pass filter for a sinusoidal input of 1 MHz.

Case 2 : Inverting, non-inverting HP and BP filter (choice No. 3)

If $V_{i2} = V_{in}$ (the input voltage signal) and $V_{i1} = V_{i3} = V_{i4} = 0$ then non-inverting high-pass (NI-HP) function is implemented at V_{o1} and inverting high pass function is obtained at V_{o3}. It may be noted that band-pass is also obtained at V_{o2}.

Figures 6 and **7** shows the frequency responses of non-inverting and inverting high pass function. The cut off frequency for the high pass function of the proposed filter circuit has been found to be 1.21 MHz. **Figure 8** shows the transient responses of non-inverting and inverting high pass functions respectively for a sinusoidal input of 10 MHz. Also the THD of non-inverting high pass function is found to be 2.3%. It may be noted that the band-pass response is not shown in this case, for brevity reasons, as it was already covered in case 1.

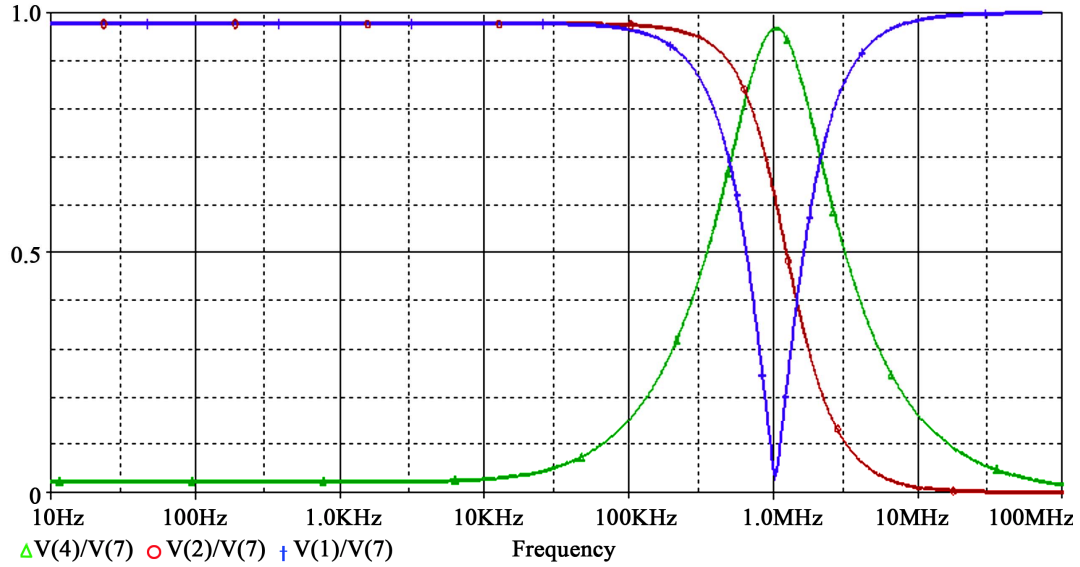

Figure 4. Frequency Response for choice no. 1.

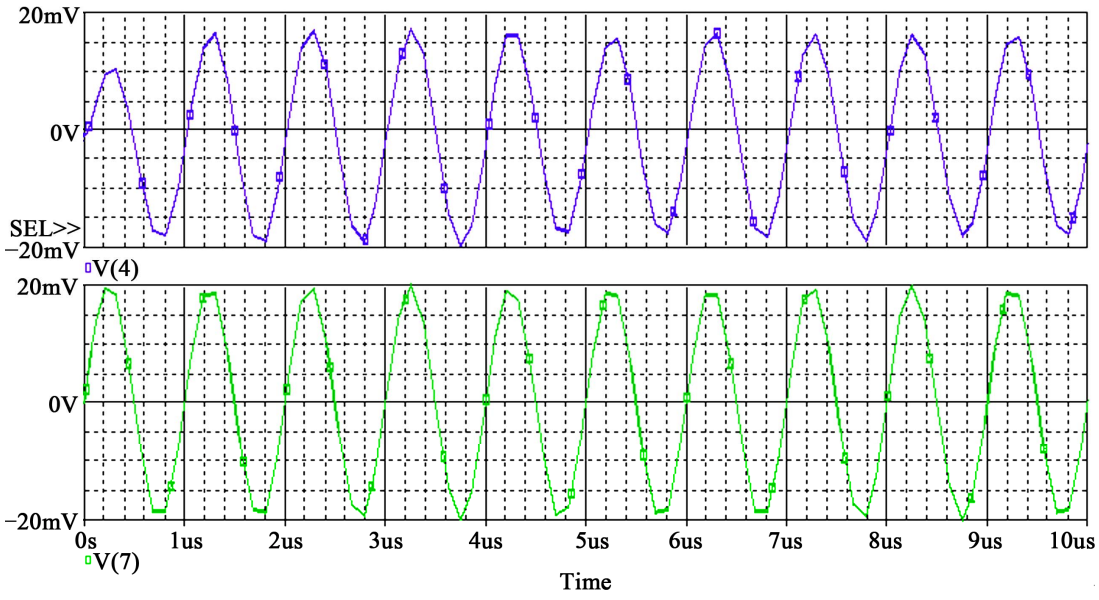

Figure 5. Input and outputs of BP filter at 1 MHz.

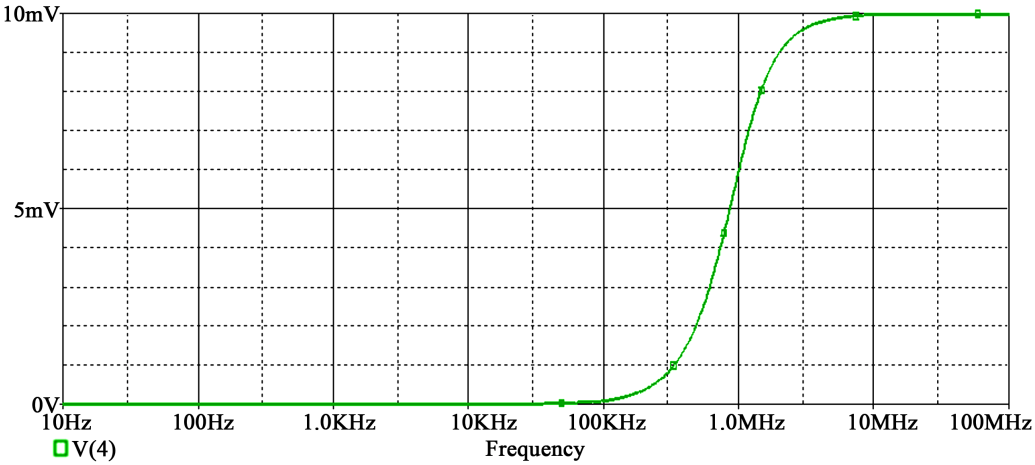

Figure 6. Frequency response of non-inverting high pass function.

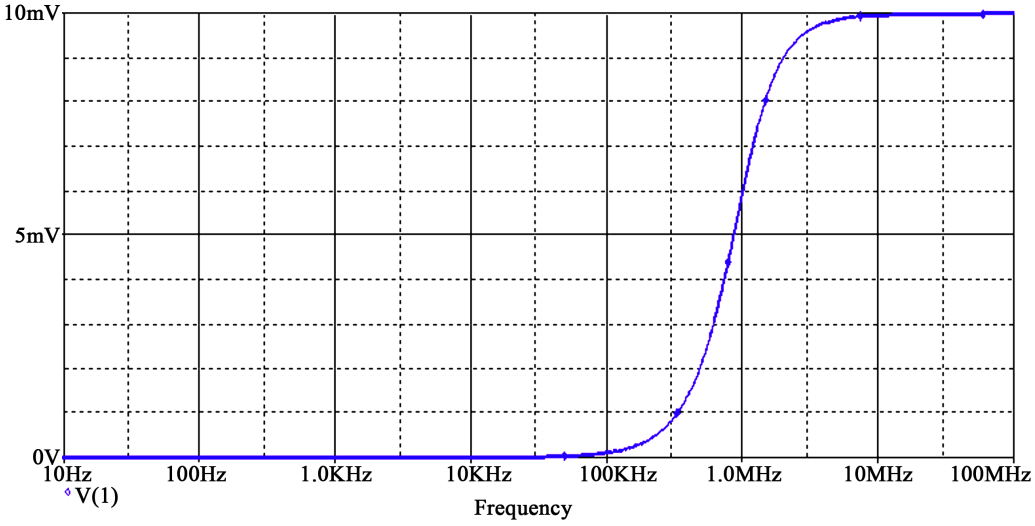

Figure 7. Frequency response of inverting high pass function.

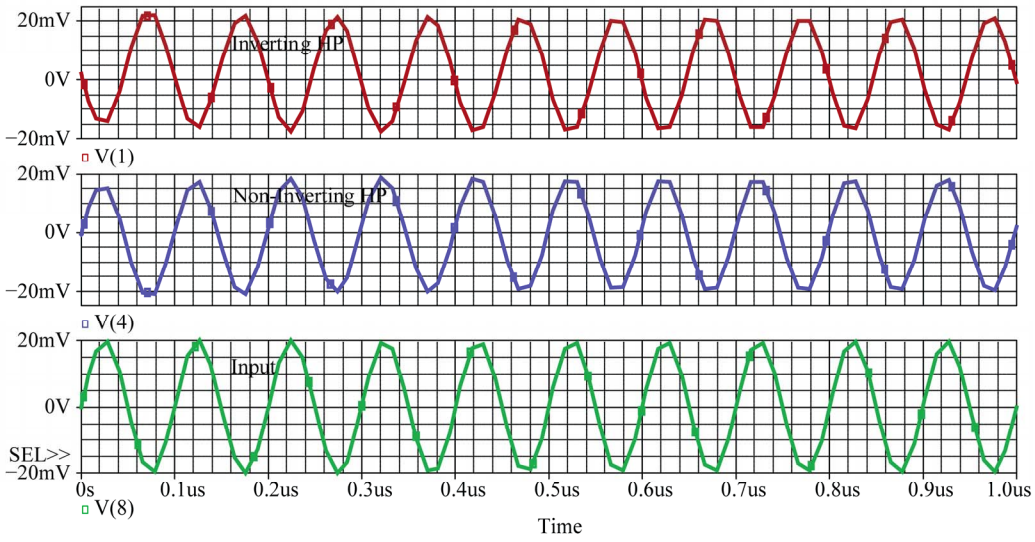

Figure 8. Input and output of HP filters at 10 MHz.

Case 3: Inverting and non-inverting all pass filter (choice No. 5)

If $V_{i1} = 0$ and $V_{i2} = V_{i3} = V_{i4} = V_{in}$ (the input voltage signal) then non- inverting all-pass (NI-AP) function is implemented at V_{o1} and inverting all-pass (I-AP) function is obtained at V_{o3}.

Figures 9 and **10** shows the frequency responses of non-inverting and inverting all pass function. **Figure 11** shows the transient responses of non-inverting and inverting all pass functions respectively for a sinusoidal input of 10 MHz.

5. Conclusions

In this paper, a novel four-input three-output voltage mode universal filter with the use of DDCC has been proposed. The circuit used three DDCCs with only two resistors and two capacitors to realize all the filter functions in inverting as well as in non-inverting form. The proposed configuration employs fewer passive components and can realize low pass, band pass, high pass, all pass and band stop functions, each with inverting and non-inverting transfer functions. Use of all grounded

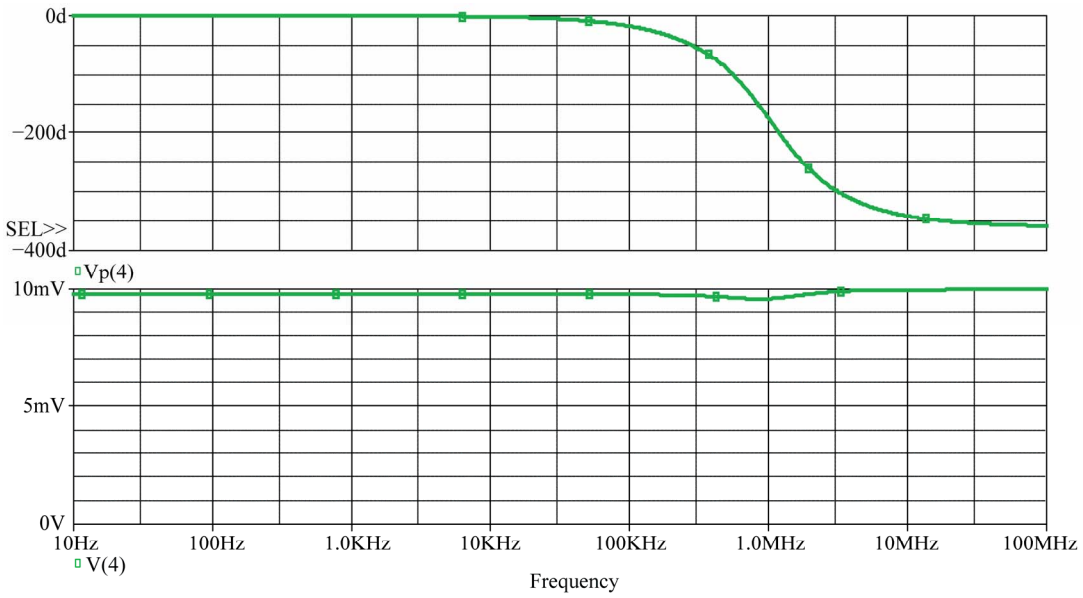

Figure 9. Gain and phase response of inverting all pass.

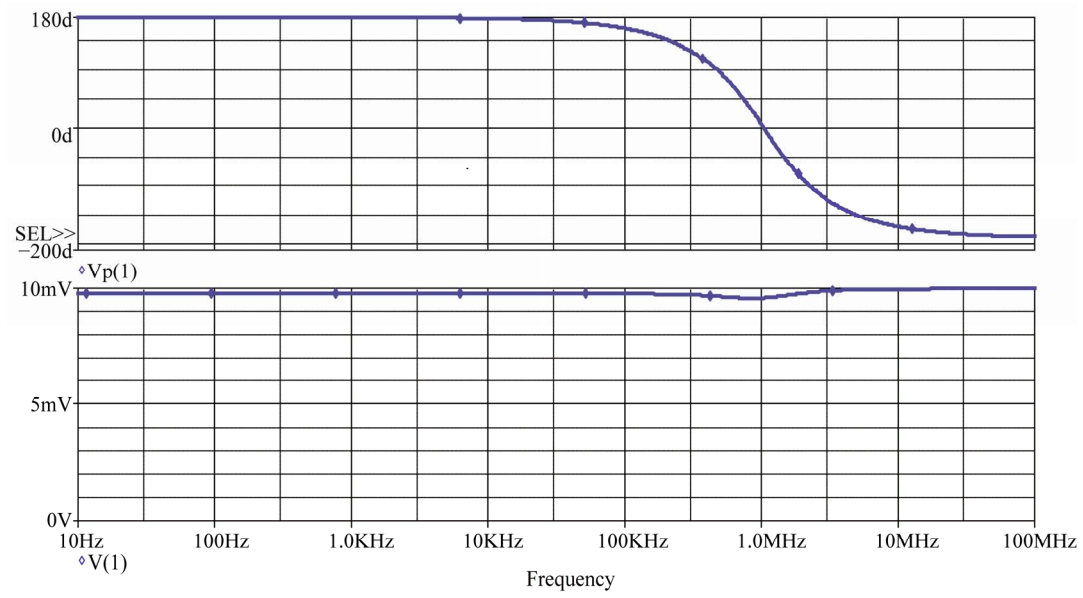

Figure 10. Gain and phase response of non-inverting all pass filter.

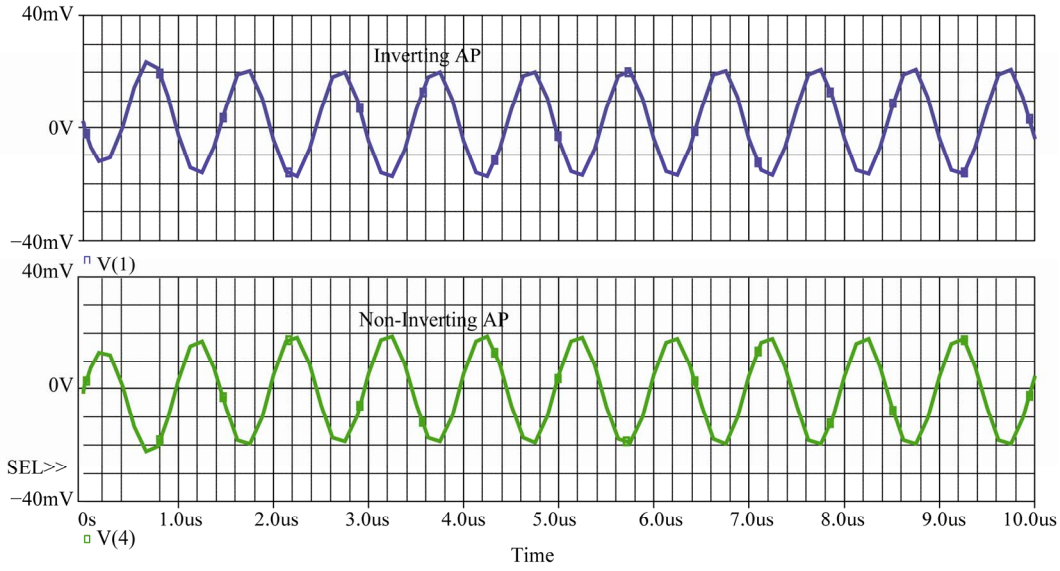

Figure 11. Transient Response of inverting and non-inverting AP functions.

passive components makes the new circuit especially attractive for IC implementation.

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