Study of Timing Characteristics of NOT Gate Transistor Level Circuit Implemented Using Nano-MOSFET by Analyzing Sub-Band Potential Energy Profile and Current-Voltage Characteristic of Quasi-Ballistic Transport

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Abstract

This paper presents the quasi-ballistic electron transport of a symmetric double-gate (DG) nano-MOSFET with 10 nm gate length and implementation of logical NOT transistor circuit using this nano-MOSFET. Theoretical calculation and simulation using NanoMOS have been done to obtain parameters such as ballistic efficiency, backscattering mean free path, backscattering coefficient, critical length, thermal velocity, capacitances, resistance and drain current. NanoMOS is an on-line device simulator. Theoretical and simulated drain current per micro of width is closely matched. Transistor loaded NOT gate is simulated using WinSpice. Theoretical and simulated value of rise time, fall time, propagation delay and maximum signal frequency of logical NOT transistor level circuit is closely matched. Quasi-ballistic transport has been investigated in this paper since modern MOSFET devices operate between the drift-diffusion and ballistic regimes. This paper aims to enable modern semiconductor device engineers to become familiar with both approaches.

Keywords

Theoretical, Simulation, Nano-MOSFET, Transistor Level, Quasi-Ballistic

1. Introduction

In traditional semiconductor devices, carriers are frequently scattered from phonons, ionized impurities and surface roughness. In the traditional devices, the backscattering mean free path λ is much shorter than the device channel. So, drift-diffusion approach is used to describe the carrier transport. However, as devices downscale to nanometer regime, backscattering mean free path become comparable to transistor dimensions. When the backscattering mean free path becomes much larger than the transistor channel length, scattering can be totally ignored. In this situation, a nano-MOSFET behaves like a vacuum tube. In practical devices, scatterings are unavoidable in semiconductor devices. Therefore, modern devices operate in quasi-ballistic mode which is between drift-diffusion and ballistic regimes. Put in other words, drift-diffusion theory is no longer strictly valid as well as ballistic treatment. Hence, modern device engineer must familiar with both approaches. Then, the nano-MOSFET studied in this paper is applied in implementing logical NOT transistor level circuit [1] [2] [3] [4].

2. Theory and Methodology

Silicon (Si) MOSFETs currently operate between the ballistic and diffusive limits; the scattering model provides a conceptual model for transport in this quasi-ballistic regime. In this scattering model, the most important scatterings occur in the low-field region near the beginning of the channel at source side. Carrier scattering in the channel reduces the current and can be described by ballistic efficiency. Scattering model predicts that the drain current is close to the ballistic limit under high drain bias than under low drain bias, and the on-state current in strong inversion is limited by a small portion of the channel near the source, that is the top region of sub-band potential barrier.

The double-gate (DG) nano-MOSFET structure used in NanoMOS simulation is shown in Figure 1 with simulation structural parameters listed in Table 1.
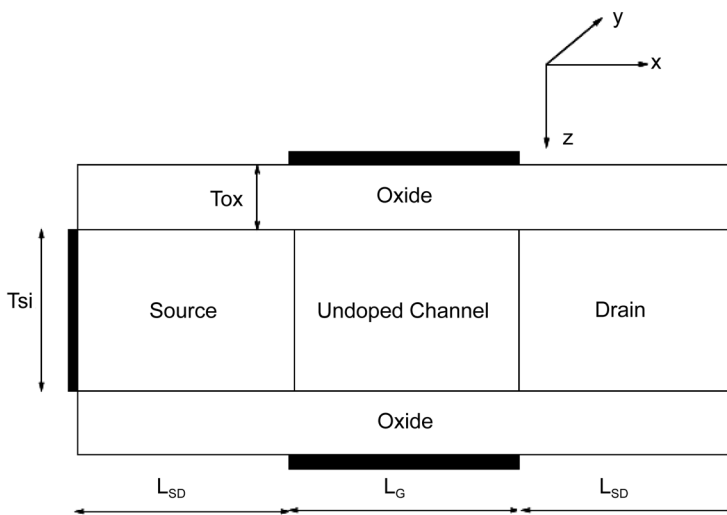

Figure 1. Structural DG Nano-MOSFET used in nanoMOS simulation tool.

Table 1. Double gate nano-MOSFET device simulation parameter.

V_{GS}	0.60 V
V_{DS}	0.60 V
V_{TO}	0.20 V
Source/drain doping concentration (N_D)	1×10^{20} cm^{-3}
Channel body acceptor impurity concentration (N_A)	1×10^{16} cm^{-3}
Channel width (W)	125 nm
Channel length (L)	10 nm
Source length/drain length (L_{SD})	7.5 nm
Silicon channel thickness (T_{Si})	1.5 nm
Top/bottom oxide insulator thickness (T_{OX})	1.5 nm
Top/bottom insulator relative dielectric constant	3.9
Channel body relative dielectric constant	11.7
Top/bottom gate contact work function	4.1888 eV

The on-state current of the nano-MOSFET is controlled by a short low-field region close to the source end of the channel. The length l of this area is called critical length which is defined as the distance from the peak of the potential barrier to the point where the potential reduces by $\beta \dfrac{k_B T}{q}$. β is a numerical factor ≥ 1. This factor has a value of 1 for non-degenerate case and slightly greater than 1 for degenerate case. In this paper, take $\beta = 1.1$. λ is the backscattering mean free path. Then, the backscattering coefficient r is given by

$$r = \frac{l}{l + \lambda}. \tag{1}$$

The ballistic efficiency B is given by

$$B = \frac{\lambda}{\lambda + 2l} \tag{2}$$

$$\lambda = \frac{2\mu}{v_T} \frac{k_B T}{q} \frac{\mathcal{F}_0(\eta_F)\mathcal{F}_0(\eta_F)}{\mathcal{F}_{-1}(\eta_F)\mathcal{F}_{1/2}(\eta_F)} \tag{3}$$

where electron mobility at ballistic transport in Silicon is $\mu = 1200$ cm^2/Vs. The thermal velocity is given by

$$v_T = \sqrt{\frac{2k_B T}{\pi m_t^*}} \tag{4}$$

where $m_t^* = 0.19 \times m_e$ and $T = 300$ K. The critical length is given by

$$l = L \left\{ \frac{\beta \left(\frac{k_B T}{q} \right)}{V_{DS}} \right\}^{\alpha}. \tag{5}$$

Since lower bound for $\alpha = 0.66$ is used at diffusive transport and upper bound for $\alpha = 0.75$ is used at ballistic transport, $\alpha = 0.705$ is used at quasi-ballistic transport.

In studying the theoretical part of this paper, the following Fermi-Dirac integrals are used:

$$\mathcal{F}_0 (\eta_F) = \ln \left(1 + e^{\eta_F} \right) \tag{6}$$

$$\mathcal{F}_{-1} (\eta_F) = \frac{1}{1 + e^{-\eta_F}} \tag{7}$$

$$\mathcal{F}_{1/2} (\eta_F) = e^{\eta_F} \tag{8}$$

where

$$\eta_F = \frac{\epsilon - E_i}{k_B T}. \tag{9}$$

ϵ is the average energy between source and drain in sub-band energy profile whereas E_i is the energy level at the center of the device. Next, the following expression is used to analyze the drain current per micron of width:

$$\frac{I_D}{W} = C_{ox} \widetilde{v_T} (V_{GS} - V_T) \left[\frac{1 - \frac{\mathcal{F}_{1/2} \left(\eta_{F1} - \frac{qV_D}{k_B T} \right)}{\mathcal{F}_{1/2} (\eta_{F1})}}{1 + \frac{\mathcal{F}_0 \left(\eta_{F1} - \frac{qV_D}{k_B T} \right)}{\mathcal{F}_0 (\eta_{F1})}} \right]. \tag{10}$$

After considering the ballistic efficiency B,

$$\frac{I_D}{W} = B C_{ox} \widetilde{v_T} (V_{GS} - V_T) \left[\frac{1 - \frac{\mathcal{F}_{1/2} \left(\eta_{F1} - \frac{qV_D}{k_B T} \right)}{\mathcal{F}_{1/2} (\eta_{F1})}}{1 + \frac{\mathcal{F}_0 \left(\eta_{F1} - \frac{qV_D}{k_B T} \right)}{\mathcal{F}_0 (\eta_{F1})}} \right] \tag{11}$$

$$C_{ox} = \frac{3.9 \times \varepsilon_o \times 2}{T_{ox}} \tag{12}$$

is the gate oxide capacitance per unit area

$$\widetilde{v_T} = \sqrt{\frac{2 k_B T}{\pi m_t^*}} \frac{\mathcal{F}_{1/2} (\eta_{F1})}{\mathcal{F}_0 (\eta_{F1})} \tag{13}$$

$$\eta_{F1} = \frac{\epsilon - E_i}{k_B T}. \tag{14}$$

ϵ is the average energy between source and drain in sub-band energy profile whereas E_i is the energy level at the region around top of the potential barrier. This region limits on-state current because scatterings mostly occur in this region. In analyzing Equation (10) and Equation (11), the following Fermi-Dirac integrals are used:

$$\mathcal{F}_{1/2}\left(\eta_{F1} - \frac{qV_D}{k_B T}\right) = e^{\eta_{F1} - \frac{qV_D}{k_B T}} \tag{15}$$

$$\mathcal{F}_0\left(\eta_{F1} - \frac{qV_D}{k_B T}\right) = \ln\left(1 + e^{\eta_{F1} - \frac{qV_D}{k_B T}}\right). \tag{16}$$

The on-line current-voltage (I-V) simulation result of NanoMOS is compared with theoretical calculation using Equation (11).

In order to calculate resistance R_{Load} of nano-MOSFET at quasi-ballistic limit, uses

$$R_{\text{Load}} = \left(\frac{V_{\text{DS}}}{I_{\text{DS}}}\right) = \frac{V_{\text{th}}}{I_{\text{on-state at linear region}} \times W}. \tag{17}$$

Since digital logic gates operate at linear portion of I-V curve. This R_{Load} is used in analyzing rise time of transistor loaded NOT gate circuit. On the other hand, the following expression is used to obtain on-state channel resistance $R_{\text{channel at on-state}}$ which is used in fall time analysis.

$$R_{\text{channel at on-state}} = \frac{1}{\mu_n C_{\text{OX}}\left(\dfrac{W}{L}\right)(V_{\text{DD}} - V_{\text{th}})} \tag{18}$$

μ_n = electron mobility at ballistic = 1200 cm^2/Vs.

C_{OX} = Oxide capacitance per unit area.

Transistor loaded NOT gate as shown in **Figure 2** is simulated using WinSpice. The simulated rise time and fall time extracted from timing diagram are compared with theoretical calculated rise time and fall time [5]-[11].

Since the nano-MOSFET operates at quasi-ballistic condition:

Gate Capacitance $= \dfrac{(3.9 \times \varepsilon_0 \times L \times W) \times 2}{T_{\text{OX}}} = C_G$

Capacitance per unit area $= 8.6 \times 10^{-4}$ F/m^2

Area Capacitance $= 8.6 \times 10^{-4} \times W \times T_{\text{Si}}$

Capacitance per unit length $= 2.4 \times 10^{-10}$ F/m

Sidewall Capacitance $= 2.4 \times 10^{-10} \times (2W + 2T_{\text{Si}})$

From **Figure 3**,

$C_\Sigma = C_G + C_S + C_D =$ Gate Capacitance + Source Capacitance + Drain Capacitance

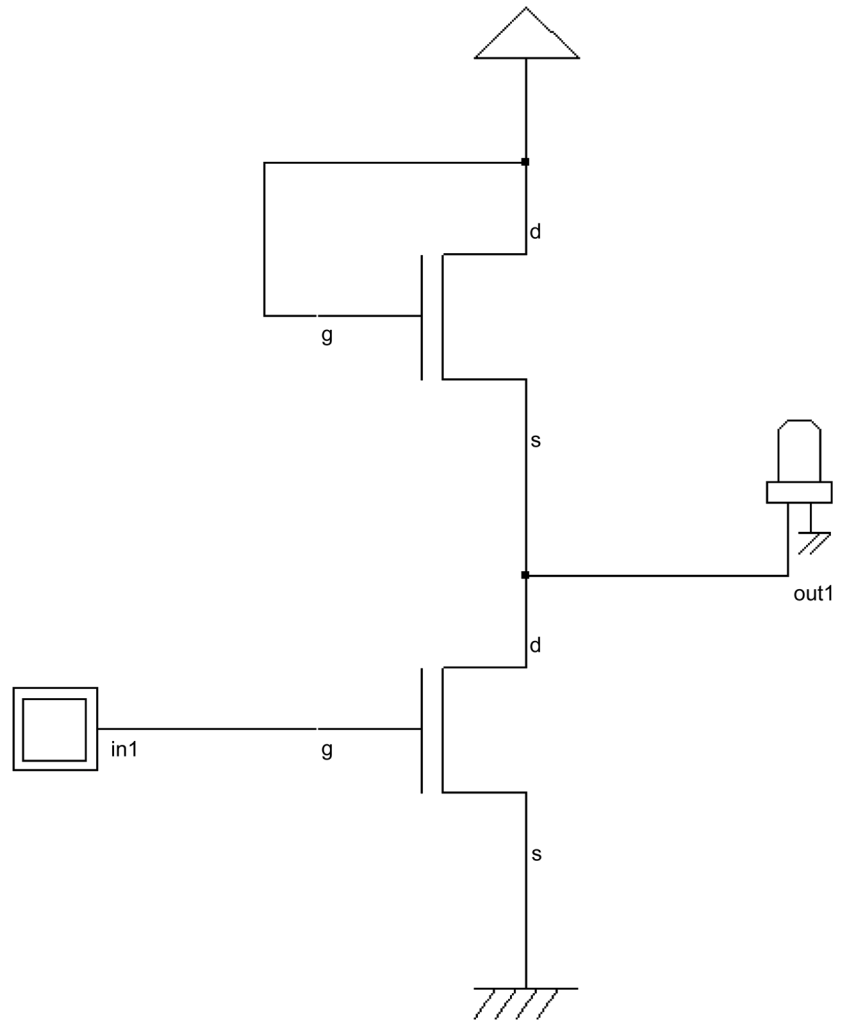$$\frac{C_G}{C_\Sigma} = \frac{2.3 k_B T / q}{S}$$

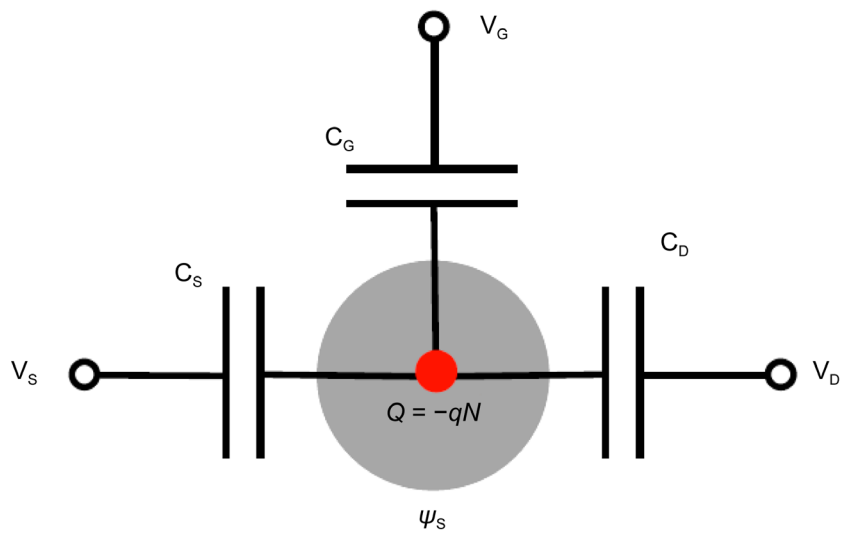**Figure 2.** Transistor loaded NOT gate circuit.

Figure 3. Capacitance models in nano-MOSFET device.

$$\frac{C_D}{C_\Sigma} = \frac{2.3k_B T}{q} \frac{DIBL}{S}.$$

From [12], subthreshold swing $S = 75$ mV/V and drain induced barrier lowering DIBL = 80 mV/dec. So, C_G, C_S and C_D can be calculated.

Total Capacitance of NOT gate = Gate Capacitance + Source Capacitance + Drain Capacitance + Area Capacitance + Sidewall Capacitance.

Rise time constant $(\tau r) = R_{\text{Load}} \times \text{NOT}$ gate total capacitance.

Rise time $(tr) = 2.2 \times \tau r \times 6.1$, it takes 6.1 times duration to pass logic 1 than logic 0 through an n-channel MOS pass-transistor.

Fall time constant $(\tau f) = R_{\text{channel at on-state}} \times \text{NOT}$ gate total capacitance.

Fall time $(tf) = 2.2 \times \tau f$.

Propagation delay $(tp) = 0.35(\tau r + \tau f)$.

Maximum signal frequency $(f_{\max}) = 1/(tr + tf)$.

3. Results and Discussion

Figure 4 shows the energy sub-band profile along the channel for nano-MOSFET studied in this paper. Drain-to-source voltage, V_{DS} lowers the sub-band potential at the drain side by 0.60 eV [13] [14] [15].

From Equation (3), the backscattering mean free path is

$$\lambda = 50.267 \text{ nm.}$$

From Equation (5), the critical length is

$$l = 1.16 \text{ nm.}$$

From Equation (1), the backscattering coefficient is

$$r = 0.02.$$

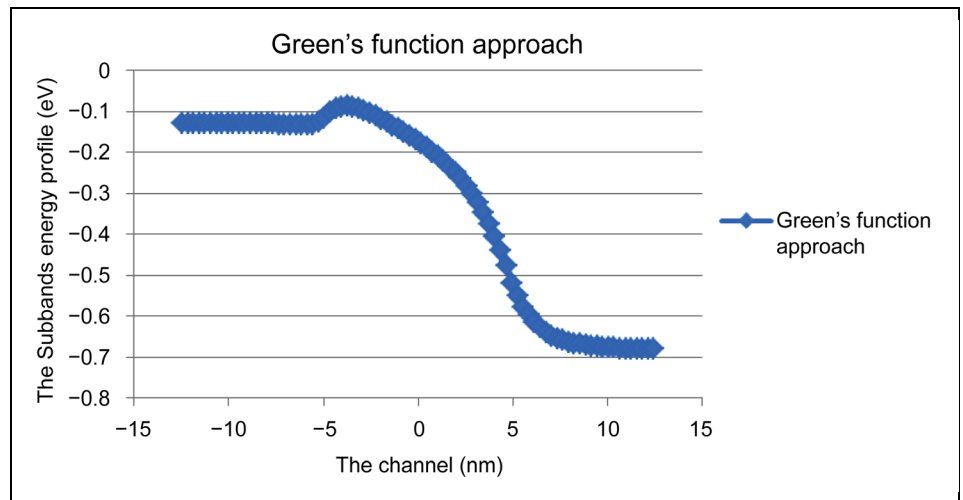From Equation (2), the ballistic efficiency is

$$B = 0.96.$$

Figure 4. The sub-band energy profile along the channel for Nano-MOSFET.

In order to analyze the NanoMOS simulation result of **Figure 5**, Equation (10) and Equation (11) are needed. Take $V_{DS} = 0.60$ V.

Then, by using Equation (10),

$$\frac{I_D}{W} = 2273.16 \ \mu A/\mu m.$$

After considering the ballistic efficiency B and using Equation (11),

$$\frac{I_D}{W} = 2182.23 \ \mu A/\mu m.$$

Simulated result with NanoMOS, as in **Figure 5**, has $\frac{I_D}{W} = 2500 \ \mu A/\mu m$. From theoretical calculation of Equation (11), $\frac{I_D}{W} = 2182.23 \ \mu A/\mu m$. These two results are 87.3% closely matched. In **Figure 5**, drain current in saturation region is sloping because electron scattering is considered in **Figure 5** and at high drain bias, scattering model in nano-MOSFET exhibits drain current closer to the ballistic limit than under low drain bias.

At region above threshold, the Fermi-Dirac integrals in Equation (11) can be simplified to exponential terms as in equation below.

$$\frac{I_D}{W} = B C_{ox} v_T \left(V_{GS} - V_T \right) \left[\frac{1 - e^{\eta_{F2} - \eta_{F1}}}{1 + e^{\eta_{F2} - \eta_{F1}}} \right] \tag{19}$$

Sub-band potential at drain side is lower by qV_{DS}, therefore

$$\eta_{F2} - \eta_{F1} = -\frac{qV_{DS}}{k_B T}.$$
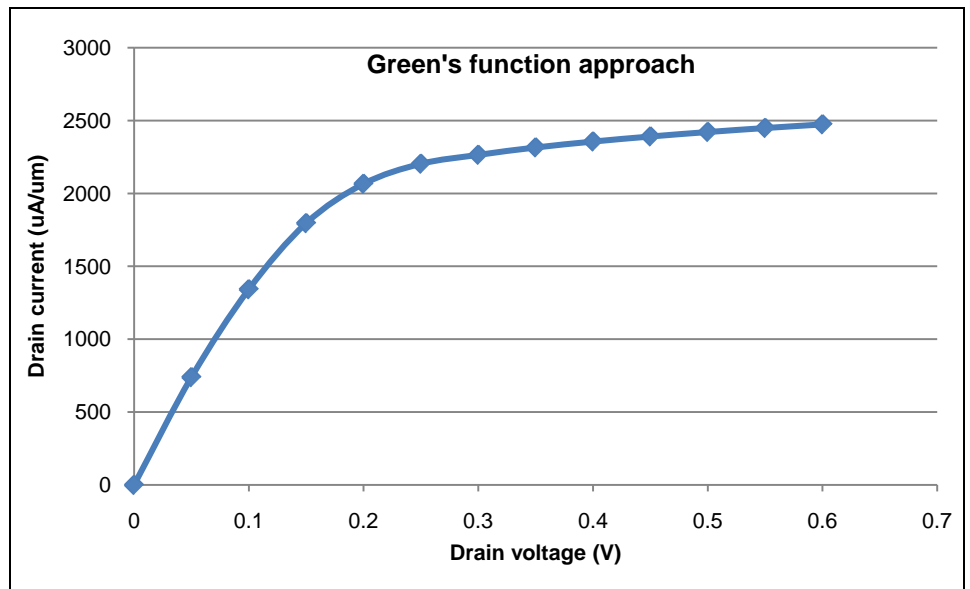
Then Equation (19) becomes

Figure 5. Drain current versus drain voltage for nano-MOSFET by NanoMOS simulation.

$$\frac{I_D}{W} = BC_{\text{ox}} v_T \left(V_{\text{GS}} - V_T \right) \left[\frac{1 - e^{-\frac{qV_{\text{DS}}}{k_B T}}}{1 + e^{-\frac{qV_{\text{DS}}}{k_B T}}} \right]. \tag{20}$$

After analysis, Equation (19) and Equation (20) both has the same value.

$$\frac{I_D}{W} = 2182.16 \ \mu A/\mu m$$

To implement transistor level NOT gate circuit as in **Figure 2**, the nano-MOSFET should operate in the linear region which is the region for digital logic operation. From **Figure 5**, linear region is from $V_{\text{DS}} = 0.00$ V until 0.20 V. Use Equation (11) to calculate the drain current at this linear region and then apply Equation (17) to calculate R_{Load} at quasi-ballistic limit. From Equation (11),

$$\frac{I_D}{W} = 2136.60 \ \mu A/\mu m. $$

In order to calculate the resistance of nano-MOSFET at quasi-ballistic limit, use Equation (17) since digital logic gates operate at linear portion of I-V curve. Using $V_{\text{th}} = 0.20$ V, $\frac{I_D}{W} = 2136.60 \ \mu A/\mu m$ and from device dimension W = 125 nm, $R_{\text{Load}} = 748.8$ Ω. The resistance value is used in analyzing theoretical value of rise time in NOT gate circuit. On the other hand Equation (18) is used to obtain the resistance needed in analyzing theoretical value of fall time in NOT gate circuit. Finally, the NOT gate circuit in **Figure 2** is simulated using WinSpice. The timing diagram result are shown in **Figure 6(a)** and **Figure 6(b)**.

Low output voltage V_{OL} of NOT transistor level circuit in **Figure 2** is given by

$$V_{\text{OL}} = \frac{R_{\text{channel at on-state}}}{R_{\text{Load}} + R_{\text{channel at on-state}}} \times V_{\text{DD}} = 27.67 \ \text{mV}. \tag{21}$$

From WinSpice simulation timing diagram **Figure 6(b)**,

$$V_{\text{OL}} \approx 9 \ \text{mV}. \tag{22}$$

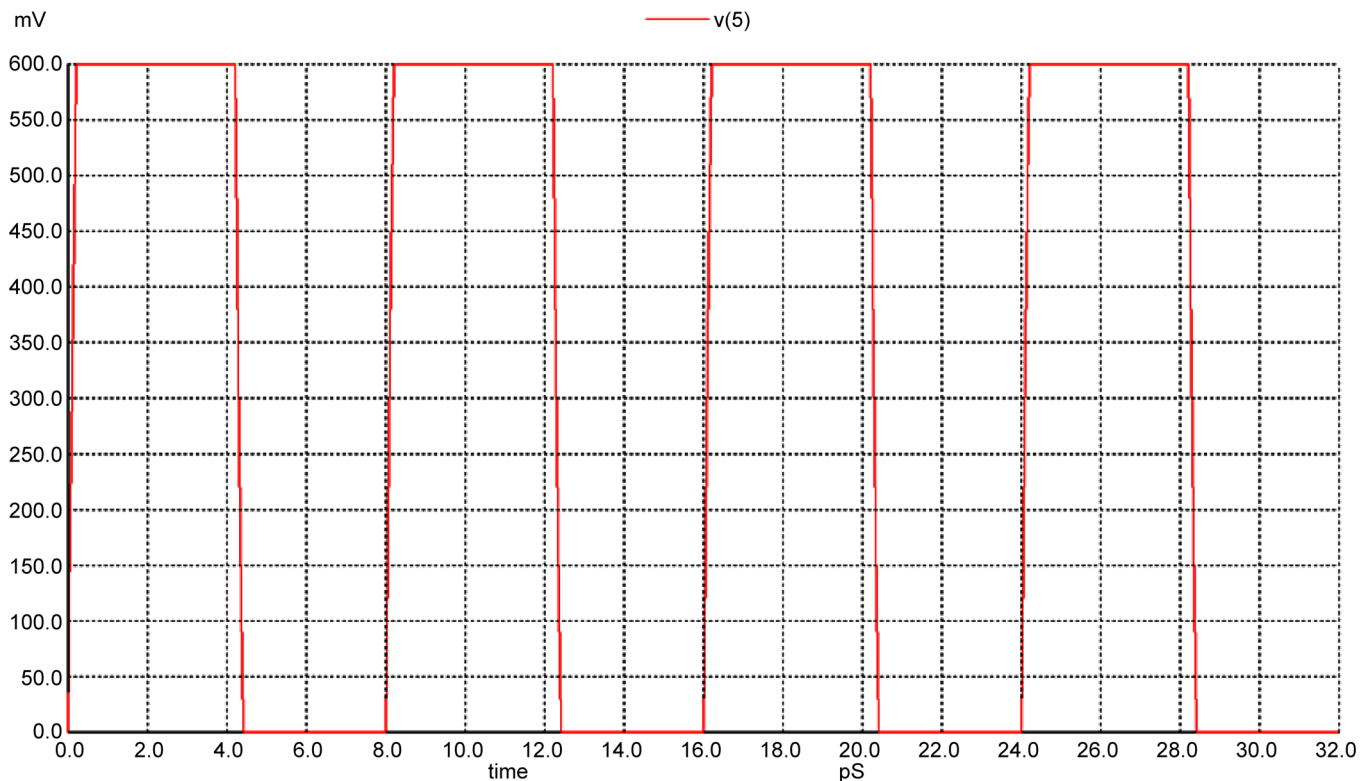By comparing Equation (21) and Equation (22),

$$\text{ratio} = \frac{27.67 \ \text{mV}}{9 \ \text{mV}} = 3.07 \ \text{times.}$$

From theoretical modeling and also WinSpice simulation, $V_{OH} = 0.4$ V. Nano-MOSFET at the bottom is at off state and thereby at high impedance state. Threshold voltage lost 0.20 V occurs at top side nano-MOSFET load which acts as pass transistor.
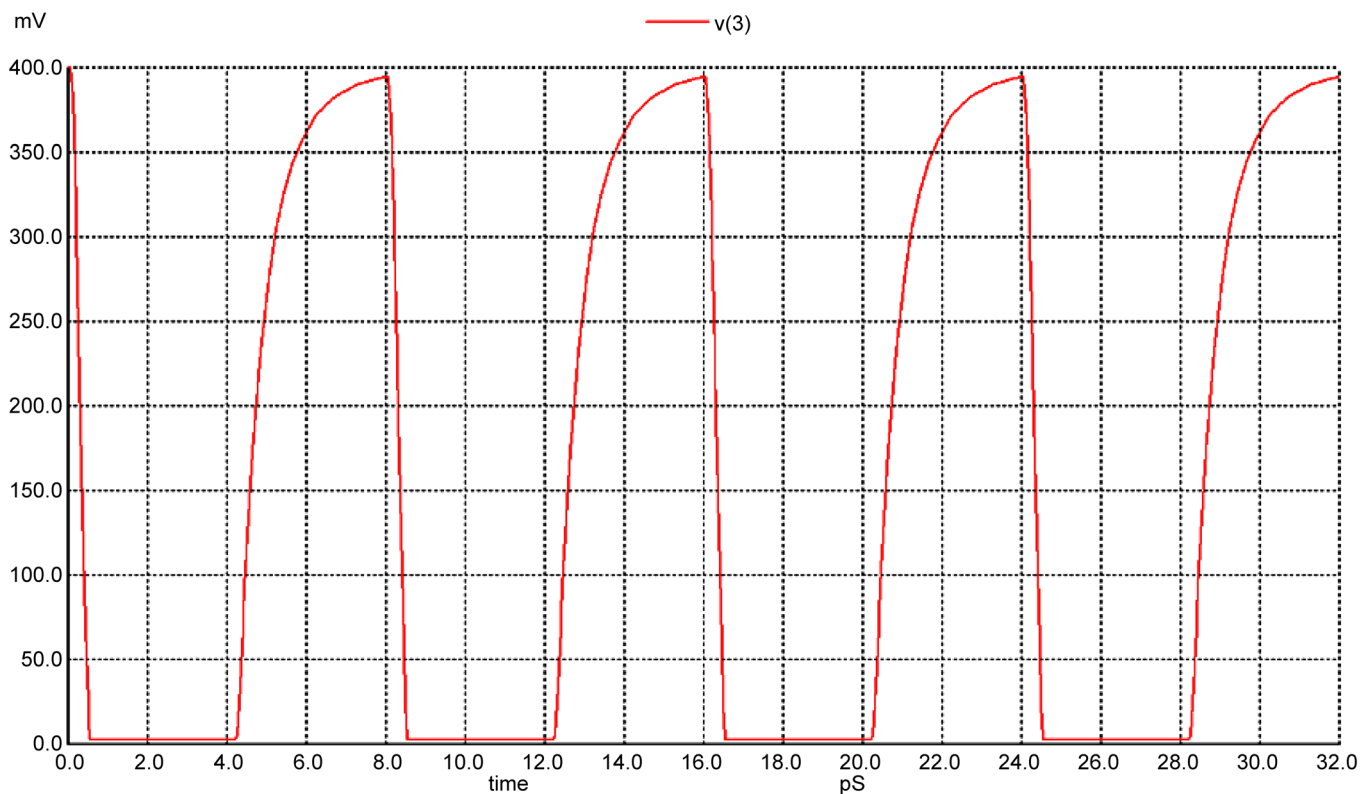
Table 2 tabulates the result of this investigation. The theoretical and simulated result are almost matched each other.

4. Conclusion

Modern MOSFET semiconductor devices operate in quasi-ballistic transport. Quasi-ballistic transport is the carrier transport between drift-diffusion and ballistic regimes.

Figure 6. (a). WinSpice input signal with period 8 ps to NOT gate; (b) WinSpice output signal of NOT gate.

Table 2. Theoretical and simulated result comparison table.

Parameters		
Gate capacitance (F)		5.7551E−17
Area capacitance (F)		1.6125E−19
Sidewall capacitance (F)		6.0720E−17
Total drain capacitance (F)		4.6041E−18
Total source capacitance (F)		1.0469E−17
NOT gate total capacitance (F)		1.3400E−16
Load resistance (ohm)		748.8
On-state channel resistance (ohm)		36.2
	Theoretical value	WinSpice simulated value
Rise time constant	9.9969E−14	1.2645E−13
Rise time (s)	1.3416E−12	1.6969E−12
Fall time constant	4.8329E−15	1.1000E−13
Fall time (s)	1.0632E−14	2.4200E−13
Propagation delay (s)	3.6322E−14	8.2756E−14
Maximum frequency (Hz)	7.3953E+11	5.1600E+11

Theoretical calculations and simulation results about this transport have been done in this paper and this paper shows that theoretical calculation values and simulation results are closely matched. Logic NOT circuit level has been implemented using nano-MOSFET and correct logical operation has been achieved.

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