A Very Low Level dc Current Amplifier Using SC Circuit: Effects of Parasitic Capacitances and Duty Ratio on Its Output

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Abstract
This paper describes a very low level dc current amplifier using switched capacitor (SC) circuit to miniaturize and improve its output response speed, instead of the conventionally used high-ohmage resistor. A switched capacitor filter (SCF) and an offset controller are also used to decrease vibrations and offset voltage at the output of the amplifier. The simulation results show that the parasitic capacitances that are distributed to the input portion of the amplifier have some effect on offset voltage. From the experimental results, it is seen that the duty ratio of the clock cycle of SC circuit should be in the range from 0.05 to 0.70. It is suggested that the proposed very low level dc current amplifier using SC circuit is an effective way to obtain both a faster output response and its miniaturization.

Keywords
dc Amplifier, Small Current Measurement, Switched Capacitor (SC) Circuit, SC Filter

1. Introduction
When very small currents are measured by mass spectrometers and radiation detectors, response speeds of the measuring instruments are limited by those of very low level dc current amplifiers [1]. This means that the amplifiers are required to observe rapid transient phenomena. In general, the very low level dc current amplifier for measuring small currents consists of an amplifier having high input impedance and a high-ohmage negative feedback resistor. The amplifier with high-ohmage resistor has unavoidable effects of the stray capacitances across its terminals. This factor causes the amplifier to have a complicated frequency characteristic, which results in its poor responses [1] [2]. Some shielding techniques [3]-[5] have been reported for the purpose of de-
increasing these capacitive components. In spite of the fact that these methods have been employed, it is difficult to realize drastic improvements of the response speeds of the very low level dc current amplifier. Neither are the amplifiers with shielding methods appropriate for miniaturization. A positive feedback circuit [6] had also been used as another approach to decreasing the stray capacitances. The amplifier with the positive feedback circuit however is unstable and begins to oscillate in this case. The resultant high speed response of the amplifier has not been achieved so far.

In this paper, an amplifier with switched capacitor (SC) circuit and offset controller are proposed. The SC circuit is equivalent to a resistor and is suitable for miniaturization. We investigated how much effect parasitic capacitances in the SC circuit have on the amplifier’s output. Furthermore, effect of duty ratio of the clock cycle on the output of the amplifier was experimentally demonstrated.

2. Circuit Analysis

2.1. Circuit Description

Figure 1 depicts a very low level dc current amplifier, including SCF and a small current source. \(C_i\), \(R_i\) and \(K\) are the input capacitance, input resistance, and amplification factor of the amplifier having a high input resistance, respectively. As an input signal to the amplifier in our experiment, we utilize a triangular wave voltage produced by the function generator \(V_g\) and the differentiating capacitor \(C_s\) (reactance attenuator) to obtain a square wave current \(I_s\) with a high output impedance. \(C_o\) is the output capacitance to the ground of \(C_i\). The input stage of the offset controller is composed of a JFET which has much higher input impedance than the negative feedback circuit has. Its voltage drift is very small (several \(\mu\)V). Therefore, the offset controller does not have much effect on the current detection sensitivity of the amplifier. The SC negative feedback circuit and SCF are shown in Figure 1(b). The former circuit is composed of a basic SC circuit and a feedback rate attenuator. The switches in Figure 1(b) are controlled by two non-overlapping clock signals. The switch \(S_{11}\) is synchronous with \(S_{12}\) and \(S_{13}\). \(S_{21}\) is synchronous with \(S_{22}\), \(S_{23}\) and \(S_{24}\). The switches \(S_{31}\) and \(S_{32}\) in the SCF are synchronous with \(S_{11}\) and \(S_{21}\), respectively.

2.2. Equivalent Resistance of SCNF

From Figure 1(b), the voltage at node \(b\), \(V_b\), is given by

\[
V_b = \frac{C_3}{C_2 + C_3} V_o
\]

and an electric charge \(q_1\) at \(C_i\) is

\[
q_1 = C_i (V_o - V_i).
\]

From Equation (1) and the relationship that \(V_o = -KV_i\), the electric charge \(q_1\) at \(C_i\) can be rewritten as

\[
q_1 = C_i \left( \frac{C_3}{C_2 + C_3} V_o + \frac{V_o}{K} \right) \approx C_i V_o \frac{C_2 + KC_3}{K (C_2 + C_3)}
\]

for \(K \gg 1\). The quantity of the charge that is transported from node \(a\) to node \(b\) is equivalent to \(q_1\) because

**Figure 1.** Circuit configurations of (a) very low level dc current amplifier; (b) SC negative feedback circuit and SCF. SC stands for switched capacitor.
the electric charge $q_1$ at $C_1$ during $T_2$ is totally discharged. Thus, a current, $I$, flowing from node $a$ into node $b$ during one clock cycle $T$ is

$$I = \frac{q_1}{T} = V_o \frac{C_1}{T} K \frac{C_2 + K C_3}{C_2 + K C_3}. \quad (3)$$

Since the current to be measured in the amplifier $I_s$ flows into the SC circuit, $I_s = I$. From the relationship that $V_o = R_{pq} I_s$, the equivalent resistance of SC negative feedback circuit $R_{pq}$ is represented by

$$R_{pq} = \frac{T}{C_1} \frac{K (C_2 + C_3)}{C_2 + K C_3} \quad (4)$$

while the equivalent SC resistance $R_{sc}$ becomes

$$R_{sc} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \quad (5)$$

where $f_s$ is the clock frequency. The attenuation factor of the attenuator $x$ is given by

$$x = \frac{C_2 + K C_3}{K (C_2 + C_3)} \quad (6)$$

Thus, from Equations (4) to (6), $R_{pq}$ can be obtained as

$$R_{pq} = \frac{1}{x C_1 f_s} = \frac{R_{sc}}{x} \quad (7)$$

It is observed from Equation (6) that $x$ is dependent on the ratio of capacitances of $C_2$ and $C_3$.

2.3. Theoretical Output Voltage of the Amplifier

The equivalent SC negative feedback circuit is illustrated in Figure 2(a). It is seen from Equations (5) and (7) that the SC negative feedback circuit is equivalent to the capacitor of $xC_1$ and four switches $S_{11}$, $S_{13}$, $S_{21}$, and $S_{24}$. The equivalent circuit of the very low level dc current amplifier is shown in Figure 2(b). The box labeled “SC” in Figure 2(b) stands for the SC negative feedback circuit. The figure shows that the equivalent SC negative feedback circuit is connected with the equivalent circuit of the amplifier at the terminals between nodes $a$ and $c$.

Applying Millman’s theorem to Figure 2(b), the input voltage $V_i$ is represented by

$$V_i = I_s + j \omega x C_1 (-K V_i)$$

and

$$C_i = C_o + C_g,$$

where $\omega$ is the angular frequency. The input admittance of the very low level dc current amplifier $Y_{in}$ is

$$Y_{in} = I_{si} + j \omega (C_i + x K C_i)$$

$$Y_{in} = I_{si} \approx \frac{1}{R_g} + j \omega (C_i + x K C_i) \quad (8)$$

Figure 2. Equivalent circuits of (a) SC negative feedback circuit and (b) very low level dc current amplifier. (c) shows simplified input equivalent circuit of (b).
for \( K \gg 1 \). Using Equation (8), a simplified input equivalent circuit of the very low level dc current amplifier using SC circuit can be drawn as shown in Figure 2(c).

An enlarged input voltage waveform of the amplifier at the positive final steady-state, \( V_i \), is illustrated with the help of clock waveform in Figure 3. \( T_s \) is the clock cycle of the switches. \( T_1 \), \( T_2 \) and \( d \) are \( (1-d)T_s \), \( dT_s \), and a duty ratio of the clock cycle, respectively. Let the input voltage of the amplifier at \( t = nT_s \) be \( V_i(n) \). Subscript symbols “+” and “−” indicate just after and just before the time event occurs, respectively. For example, \( V_i(n+1)_− \) means the voltage just before \( t = (n+1)T_s \). The amplitude of the input voltage for a cycle, \( V_m \), is

\[
V_m = \frac{1}{C_i + xKC_i} \int_{(n+1)-d/T_s}^{(n+1)/T_s} I_i dt + \frac{1}{C_i} \int_{(n+1)-(d+1)/T_s}^{(n+1)/T_s} I_i dt = \frac{C_i + dxKC_i}{C_i(C_i + xKC_i)} I_i T_s.
\]

(9)

Since electric charges of the SC circuit are conserved just before and after \( t = nT_s \), the following equation is obtained

\[ C_i V_i(n) = (C_i + xKC_i) V_i(n+1)_−. \]

The input voltage just before \( t = nT_s \) is

\[ V_i(n)_− = \left(1 + \frac{xKC_i}{C_i}\right) V_i(n). \]

(10)

From Figure 3 and Equation (10), the voltage \( V_m \) is

\[ V_m = V_i(n)_− - V_i(n) = \frac{xKC_i}{C_i} V_i(n). \]

(11)

From Equations (9) and (11), the input voltage just after \( t = nT_s \) is given by

\[ V_i(n)_+ = \frac{I_i T_s}{xKC_i} + \frac{C_i + dxKC_i}{C_i + xKC_i} I_i T_s. \]

(12)

The resultant peak voltage \( V_{ip1} \) during \( T_1 \) is

\[ V_{ip1} = V_i(n)_− + \frac{1}{C_i + xKC_i} \int_{(n+1)-d/T_s}^{(n+1)/T_s} I_i dt = V_i(n)_+ + \frac{1-d}{C_i + xKC_i} I_i T_s. \]

(13)

Substituting Equation (12) into Equation (13) gives the following equation:

\[ V_{ip1} = \frac{I_i T_s}{xKC_i} = \frac{R_{eq}}{K} I_s. \]

(14)

Therefore, the peak output voltage of the amplifier during \( T_1 \), \( V_{op1} \), can be written as

\[ V_{op1} = -KV_{ip1} = -R_{eq} I_s. \]

(15)
It is found from Equation (15) that the theoretical output voltage of the very low level dc current amplifier using SC circuit can be obtained by sampling $V_{opt}$. In this paper, the SCF is used to sample $V_{opt}$ from the output voltage of the very low level dc current amplifier using SC circuit for the following reasons. Using a sample-and-hold circuit generally requires a clock generator that completely differs from two non-overlapping clock signals utilized by the SC negative feedback circuit. Using a low-pass filter provides for not theoretical output voltage, but approximately half amplitude of output voltage of the amplifier at a final steady-state. On the other hand, using the SCF with the SC circuit allows for sharing the two non-overlapping clock signals. In addition, both the SCF and SC circuit can be manufacturable by the same process. We are easily available to miniaturize SC circuits using IC-compatible techniques. Therefore, the SCF is useful from the viewpoint of miniaturization.

3. Methods

3.1. Effect of Parasitic Capacitances on the Amplifier’s Output

To evaluate response speed of the very low level dc current amplifier, a square wave current $I_s$ with a time period of 5 ms and an amplitude of 10 nA was input to the amplifier. $K$ and $C_s$ were set to 1300 and 17 pF, respectively. We fixed the equivalent SC resistance $R_{eq}$ of 1 MΩ using $C_1$ of 10 pF and $f_s$ of 100 kHz. The attenuation factor $x$ of 1/100 was also set using both $C_2$ of 1000 pF and $C_1$ of 9.3 pF. The total equivalent resistance $R_{eq}$ of the SC negative feedback circuit was 100 MΩ. The duty ratio $d$ of 0.5 was used. A switch model [9] used in the computer simulation is shown in Figure 4. The symbols $D$, $G$, and $S$ stand for drain, gate, and source of MOS-FETs. Assuming that parasitic capacitances between two terminals exist, as shown in Figure 4(a) and Figure 4(b), each analog switch composed of a combination of an nMOS and pMOS was used (see Figure 4(c)). Transient analyses of the very low level dc current amplifier using SC circuit were carried out using the electronic circuit simulator PSpice (Cadence Design System, Inc.). Table 1 lists the parasitic capacitance values determined by trial and error.

3.2. Effect of Duty Ratio on the Amplifier’s Output

The amplification factor $K$ of the very low level dc current amplifier using SC circuit shown in Figure 1 was set to 62.3 dB. Its output waveform was observed using an oscilloscope. Since the triangular wave voltage, which had a time period of 10 ms and an amplitude of 10 V, was differentiated by the differentiating capacitor $C_s$ of 1.25 pF, a square wave current with a time period of 10 ms and an amplitude of 10 nA was obtained as an input current $I_s$ to the amplifier. As switches for the SC circuit and SCF, we used CMOS analog switches.

Figure 4. Switch model used in PSpice simulation. Configurations of (a) nMOS, (b) pMOS FET models with parasitic capacitances, and (c) CMOS switch.

Table 1. Parasitic capacitance values based on the assumption that nMOS and pMOS have the same parasitic capacitive components.

<table>
<thead>
<tr>
<th>Parasitic capacitance [pF]</th>
<th>$C_{dgn}$, $C_{gsn}$</th>
<th>$C_{dgp}$, $C_{gsp}$</th>
<th>$C_{dsn}$, $C_{subn}$</th>
<th>$C_{dsn}$, $C_{subp}$</th>
<th>$C_{gsn}$, $C_{subp}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.0</td>
<td>0.9</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
</tr>
</tbody>
</table>
(MAX326, MAXIM Integrated Products, Inc.) having the maximum leakage current of 10 pA. Further, variable capacitors $C_1$ and $C_3$ were utilized. Parasitic capacitances of analog switches have some effect on equivalent resistance of the SC negative feedback circuit $R_{eq}$, which causes errors in $R_{eq}$ of the amplifier. Thus, the equivalent SC resistance $R_{eq}$ with the clock frequency $f_c$ of 100 kHz was set to 1 MΩ by adjusting capacitance of $C_1$, and then the attenuation factor of the attenuator $x$ was set to 1/100 by adjusting capacitance of $C_3$. Referring to Equation (7), the total equivalent resistance of the SC circuit became 100 MΩ. An offset voltage controller, which was connected to the input of the amplifier and had a gain of unity, was also used to cancel the offset voltage in our experiment.

4. Results and Discussions

4.1. Effect of Parasitic Capacitances on the Amplifier’s Output

First, based on the assumption that nMOS has exactly the same parasitic capacitances as pMOS has, transient analyses of the amplifier were done. Figure 5 shows the simulation result with the parasitic capacitances shown in Table 1. It can be observed that the output waveforms of the amplifier have vibrations that cause black area due to charge and discharge actions of the SC negative feedback circuit (see Figure 5(a) and Figure 5(b)). Thus, it is difficult to measure an input current from them. Calculating average values of $V_{\text{op}}$ from 10.0 ms to 12.5 ms and from 12.5 ms to 15.0 ms in Figure 5(a), they are respective +1.0 V and –1.0 V. From Equation (15), output voltage of 1 V should be obtained as the theoretical output of the amplifier. The output waveform of the SCF, $V'_{o}$, is shown in Figure 5(c). In this case, the peaks of the output voltage during $T_i$ were sampled by the SCF. As generally defined, the rise time is the time required for the output waveform to rise from 10% to 90% of its final steady-state value. The rise time of the output waveform of the SCF is 10.3 μs, while that of the amplifier using conventionally used high-ohmage resistor is 83.8 μs [10]. It is seen from Figure 5(c) that using the
SCF considerably reduces vibrations as well as unnecessary components, and that the input current $I_s$ can be obtained by measuring the amplitude of its output voltage.

Secondly, we also performed computer simulations with an addition of 0.5 pF to each parasitic capacitance of nMOS or pMOS listed in Table 1 to find out which parasitic capacitance would have effect on the output of the amplifier. Table 2 summarizes parasitic capacitances that have effect on offset voltage of the amplifier. For example, all the cases in the switch $S_{11}$ that $C_{dg-n} (1.5 \text{ pF}) > C_{dg-p} (1.0 \text{ pF})$, $C_{dg-p} (1.5 \text{ pF}) > C_{dg-n} (1.0 \text{ pF})$, $C_{gs-n} (1.4 \text{ pF}) > C_{gs-p} (0.9 \text{ pF})$, and $C_{gs-p} (1.4 \text{ pF}) > C_{gs-n} (0.9 \text{ pF})$ cause generation of offset voltages at the amplifier’s output. On the other hand, parasitic capacitances that are not listed in Table 2 do not have effect on its output voltage. From the simulation results, it is found that differences between value of $C_{dg-n}$ and that of $C_{dg-p}$ in $S_{11}$, $S_{12}$, $S_{21}$, $S_{22}$, and $S_{23}$, and between that of $C_{gs-n}$ and that of $C_{gs-p}$ in $S_{11}$ result in generating offset voltages of the amplifier, and that parasitic capacitive components that are distributed close to the amplifier’s input portion are deeply related to it.

### 4.2. Effect of Duty Ratio on the Amplifier’s Output

Experimental results are shown in Figure 6. In the experimental result with the duty ratio of $d = 0.05$, the output amplitude of the amplifier is larger than 1 V. It is also observed that the output waveform at positive and negative final steady-states is rather distorted. On the other hand, in that of $d = 0.70$, the amplitude becomes smaller than 1 V. It is found from the experimental results that the duty ratio of the clock cycle should be in the range: $0.05 < d < 0.70$. Using duty ratios larger than 0.70 leads to output waveform degradation. It is thought that the longer $T$ (the shorter $d$) we use, the more stable output waveform can be sampled using the SCF.

Finally, a relationship between the clock frequency $f_s$ and error rate of $R_{eq}$ was investigated. Setting $f_s$ and $C_2$ to respective 100 kHz and 1000 pF, we adjusted both capacitances of $C_1$ and $C_3$ to precisely obtain $R_{eq}$ of 100 MΩ, and then changed $f_s$ ranging from 50 kHz to 200 kHz when $I_s = 5 \text{ nA}$, $I_s = 10 \text{ nA}$, and $I_s = 20 \text{ nA}$, respectively. The equivalent resistance of $R_{eq}$ was obtained by measuring output voltage of the SCF. The relationship between $f_s$ and error rate of $R_{eq}$, with $x$ of 1/100, is shown in Figure 7. Referring to Equation (7), $R_{eq}$ is inversely proportional to $f_s$. This means that decreasing $f_s$ is equivalent to increasing $R_{eq}$. It is seen from Figure 7 that there is a tendency for the error rate to decrease as $R_{eq}$ increases. It is thought that the stable output waveform will get longer as $T_s$ increases because of charge action of the SC circuit.

![Figure 6](image_url)

Figure 6. Output waveforms of the SCF with duty ratios of (a) $d = 0.05$; (b) $d = 0.10$; (c) $d = 0.50$; and (d) $d = 0.70$, respectively. Scale: H: 2.5 ms/div, V: 0.5 V/div.
5. Conclusion

It is found from the simulation results that the parasitic capacitive components that are distributed close to the input portion of the amplifier have effect on the offset voltage. The experimental results show that the duty ratio of the clock cycle has an effective range. The error rate of less than 3.0% in $R_{eq}$ is also obtained in our experiment. These results suggested that the proposed amplifier using SC circuit would provide the measuring device having better properties of both faster response and downsizing.

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References


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