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Efficient Choice of a Multilevel Inverter for Integration on a Hybrid Wind-Solar Power Station

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Abstract

DC/AC converters are very important components that have to be chosen efficiently for each type of power station. In this article, we present in details, a comparison between three different architectures of multilevel inverters, the flying capacitor multilevel inverter (FCMLI), the diode clamped multilevel inverter (DCMLI), and the cascaded H-bridge multilevel inverter (CHMLI). Thus the comparison is focused on the output voltage quality, the complexity of the power circuits, the cost of implementation, and the influence on a power bank inside the renewable power station. We also investigate trough simulation the efficient number of levels and suitable characteristics for the CHMLI that showed the most promising performance. The study uses Matlab Simulink platform as a tool of simulation, and aim to choose the most qualified inverter, for a potential insertion on a hybrid renewable energy platform (wind-solar). In all the simulations we use the same PWM control type (SPWM).

Keywords

Multilevel Inverters, FCMLI, DCMLI, CHMLI, Hybrid Power Station, SPWM, Power Bank

1. Introduction

Multilevel inverters have emerged, as a new option for DC/AC conversion [1] for high power and renewable energy applications [2] [3]. The multilevel inverter synthesizes basically a stair wave voltages staged in several DC levels [4]. There are many topologies of multilevel inverters, some are basic, others are a combination of different types, and however they can be classified into three basic structures: the FCMLI, the DCMLI, and the

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CHMLI. All multilevel inverter topologies produce almost a similar output, which consists of voltage steps, thus providing a higher quality voltage [5], compared to classic 2 level inverters, and as close as possible to the waveform intended to be produced. Multilevel inverters are an efficient alternative to solve problems posed by conventional inverters; their main characteristics are having lower switching losses, lower solicitation on switching devices, higher power applications, and they filter easier since the output consists of DC voltage levels. In literature, there are many research activities dealing with a special topology trying to raise the number of levels [6], or developing new methods for harmonic minimization [7] [8]. In this paper we decided to focus our study on the three 5 level basic multilevel inverters, as they are the most widespread [9], and investigate the most efficient parameters for the CHMLI, as it was the best candidate in our comparative study. An analysis using Matlab Simulink tool was made, to compare between the performances of the different 5 levels architectures (voltage quality, the complexity of the power circuits, the cost of implementation [10], and the impact on a power bank inside the renewable power station) using the same PWM techniques [11] in order to choose the best inverter suited for a hybrid wind-solar renewable power station. An evaluation of the effect of levels configuration on the CHMLI performance was made to determinate the most effective parameters of this inverter. Thus a simulative testing of the CHMLI inverter was made from level 5 to 15.

2. The Hybrid Renewable Power Station with a Classic Inverter

The hybrid renewable power station that the inverter is intended to, is composed basically of two sources; photovoltaic panels and a wind turbine. In this part we simulate the work of the power station, with a normal full bridge inverter, in order to compare its performance to the rest of multilevel inverters. The **Figure 1** presents the diagram used on Matlab Simulink to simulate the running of the inverter.

Figure 2 represents the wave form of the output voltage, and current of the full bridge used in the simulation. The output current of the full bridge inverter was simulated with a (R = 50 Ω, L = 100 mH) load.

The total harmonic distortion is given by the well-known expression:

$$THD = \frac{\sqrt{\sum_{k=2}^{n} V_k}}{V_1} \tag{1}$$

V_k is the k harmonic and V_1 is the fundamental. The **Figure 3** shows the output voltage spectrum; we found that the classic full bridge inverter that we used has an output voltage THD of 76.51%, which is very high compared to the signal purity wanted in the hybrid power station.

In the power bank where we used a model of 20 lead acid batteries of 12 Vdc, and a rated capacity of 6.5 Ah each, we noticed a general power drop of 57.3 mv during a 1 sec time simulation.

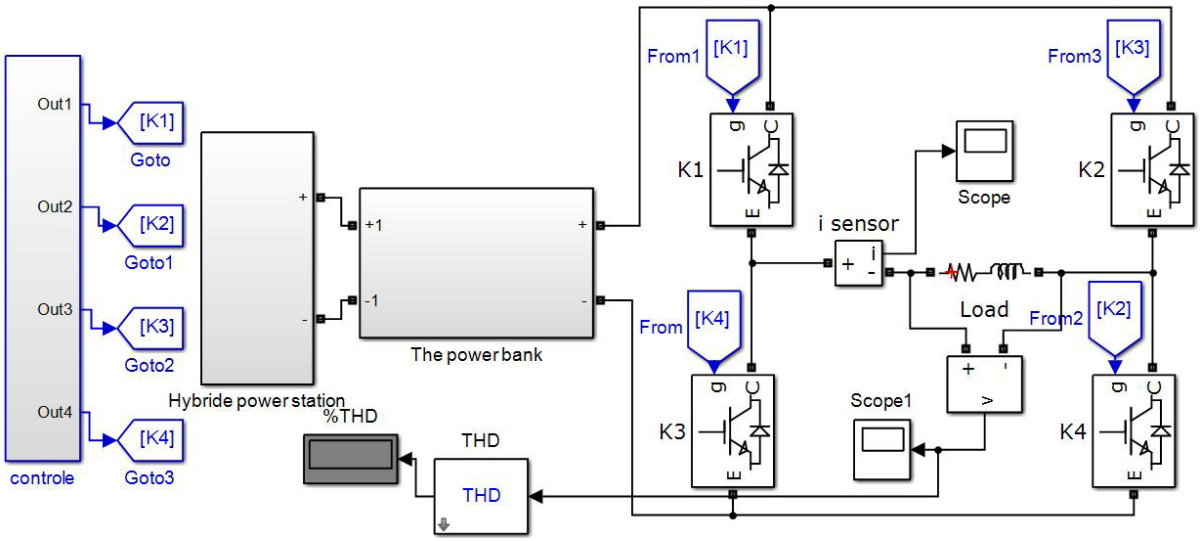


Figure 1. Diagram of the full bridge inverter used on Matlab Simulink.

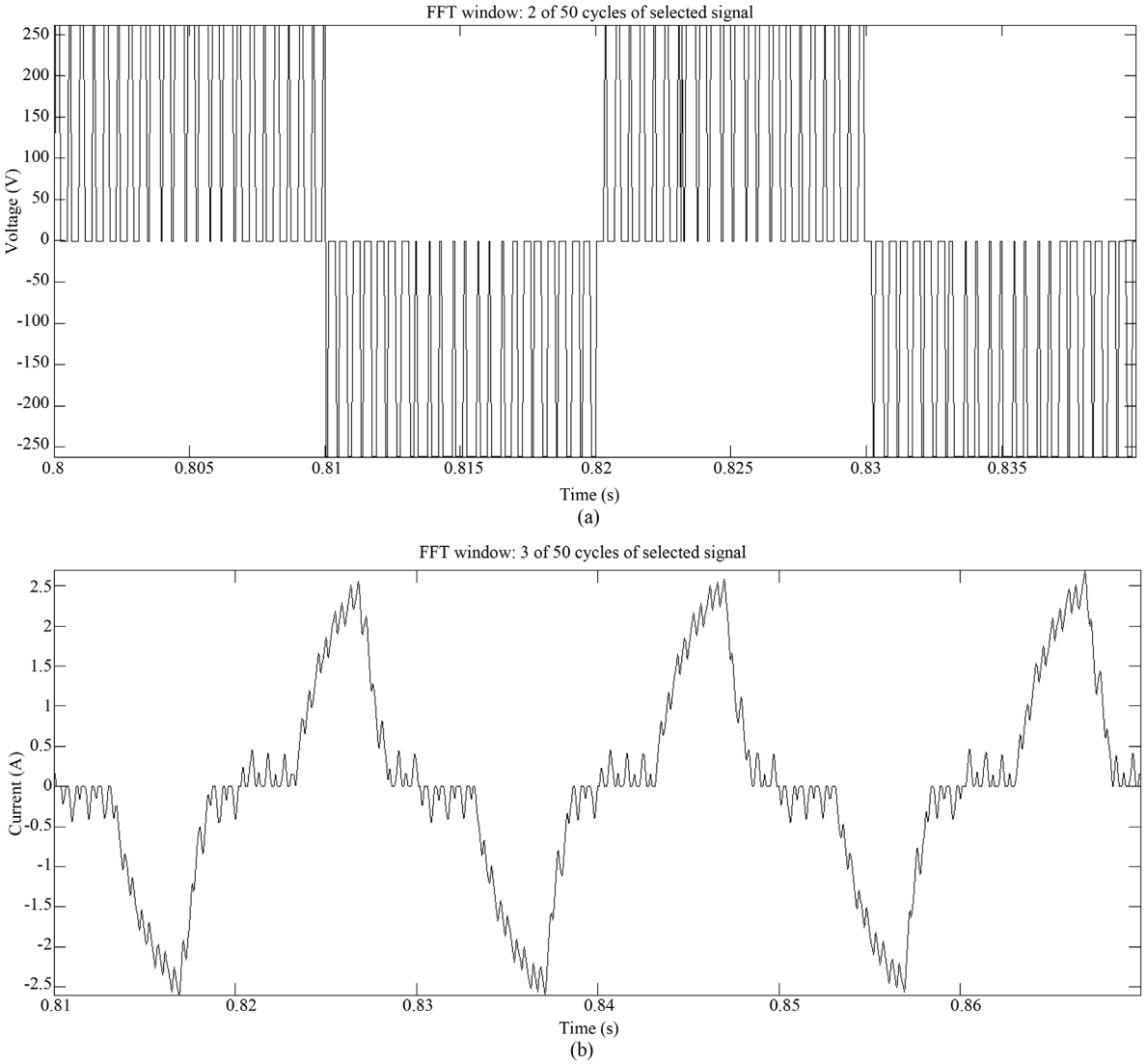


Figure 2. Output simulation results of the full bridge: (a) voltage; (b) current.

3. The Hybrid Renewable Power Station with the Studied Multilevel Inverters

3.1. The PWM Law Command and Power Bank Used for All Multilevel Inverters in the Simulation

In this entire article we used the same SPWM law command, which is the most widespread command in multilevel inverters field. Its principle is to compare a reference signal V_{ref} to four saw tooth carriers **Figure 4**.

The signal references for the three phases used in the simulation are expressed as follows:

$$V_{1ref} = A \cdot m \cdot \sin(wt) \tag{2}$$

$$V_{2ref} = A \cdot m \cdot \sin\left(wt - \frac{2\pi}{3}\right) \tag{3}$$

$$V_{3ref} = A \cdot m \cdot \sin\left(wt - \frac{4\pi}{3}\right) \tag{4}$$

$A = 10$: The magnitude.

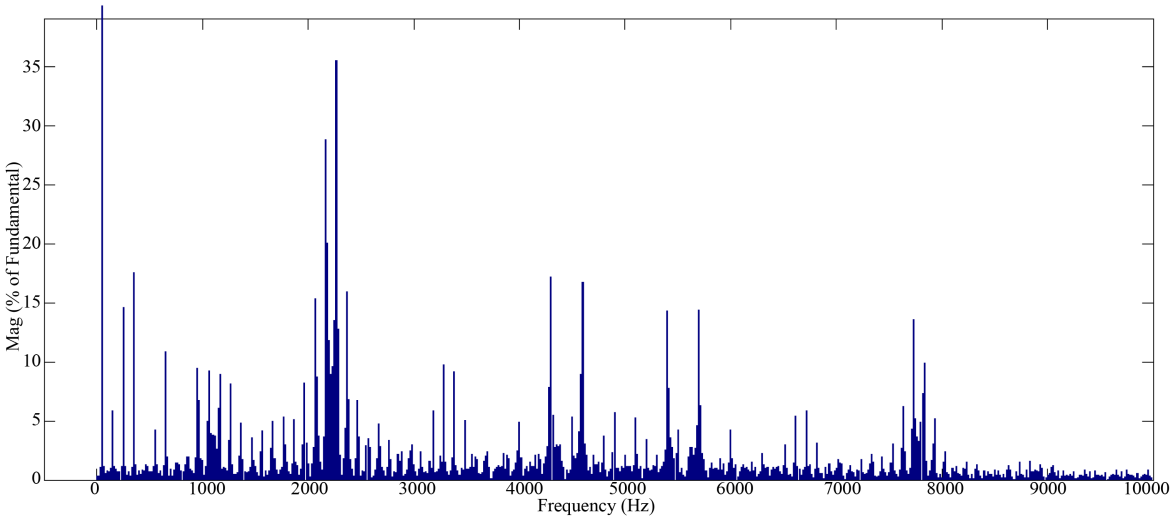


Figure 3. Output voltage spectrum analyze of the full bridge inverter.

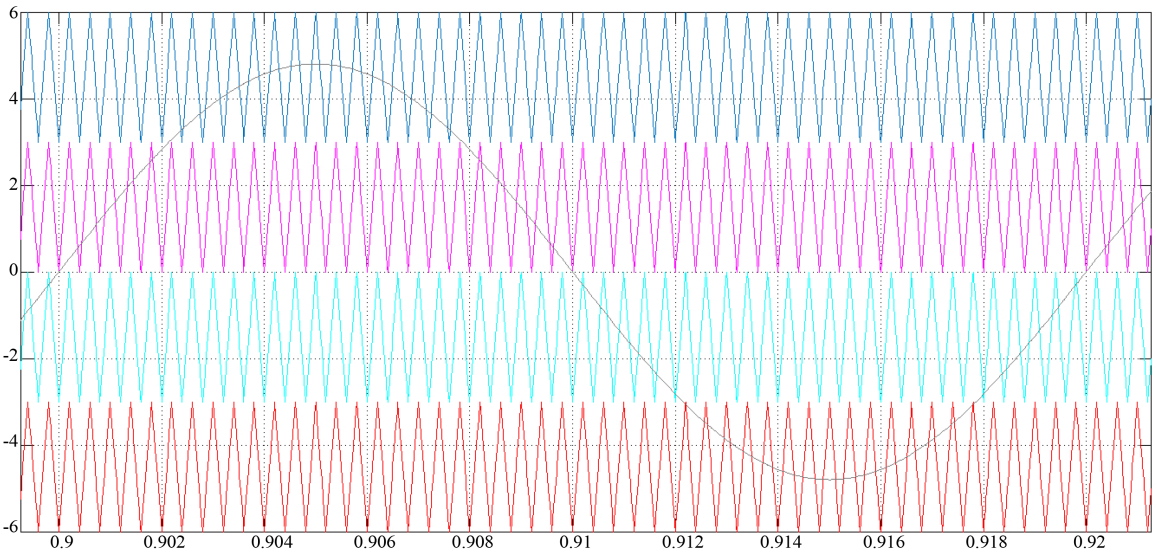


Figure 4. The reference signal with the four saw tooth carriers used for the command.

$m = 0.6$: The modulation index.

$f = w/2\pi$: The frequency.

In order to see the influence of each multilevel inverter on storage units, we modeled a power bank out of 20 lead-acid batteries on Matlab Simulink having the following simulation characteristics:

- Nominal voltage: 12 V
- Rated capacity: 6.5 A·h
- Initial state of charge: 100%
- Maximum capacity: 6.77 A·h
- Fully charged voltage: 13.06 V
- Nominal discharge current: 1.3 A
- Internal resistance: 0.02 Ω

3.2. The Flying Capacitor Multilevel Inverter (FCMLI)

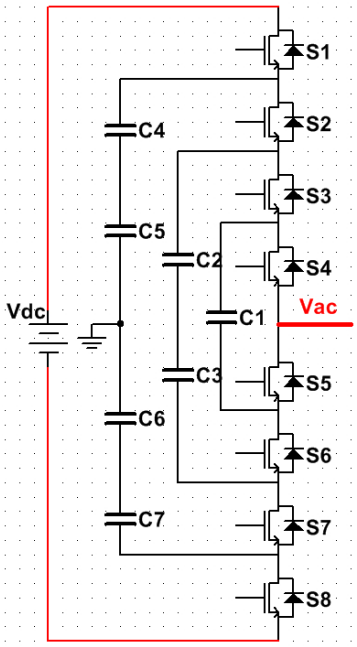
In this type of multilevel inverters, the output can be expressed as the different possible combinations of

connection of the capacitors [12]. This structure is similar to the DCMLI but uses capacitors instead of diodes to set the voltage levels.

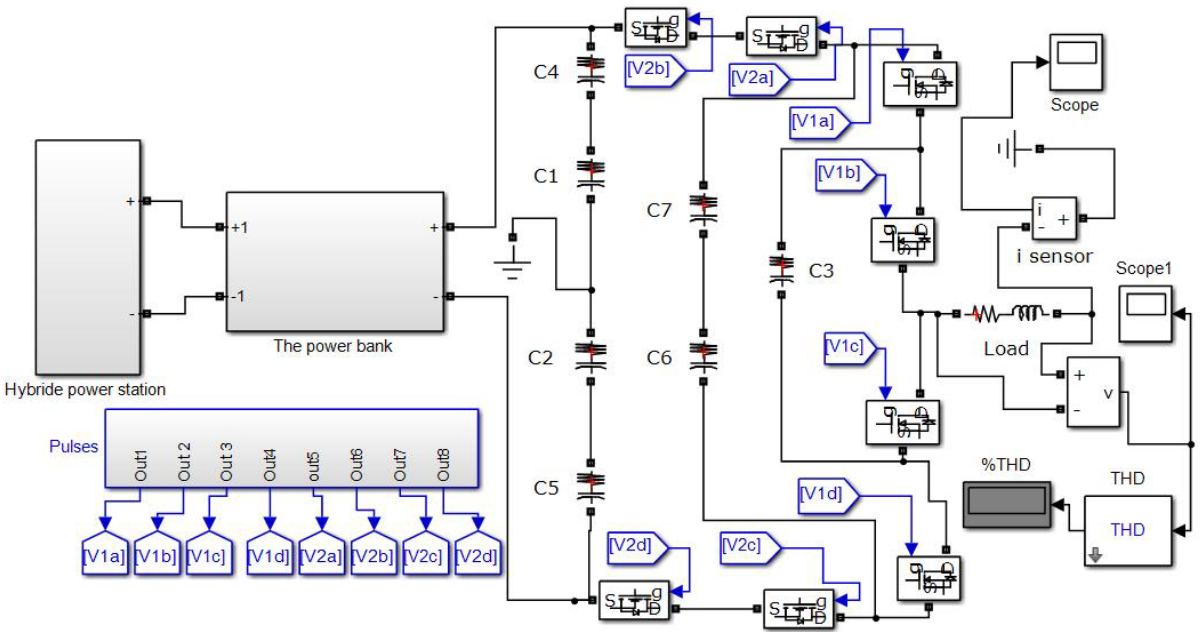
If we examine the power circuit of the FCMLI **Figure 5(a)** we can find some useful relations; if m is the number of levels, *k* the number of capacitors at the DC side, l the number of switches per phase, and N_c the number of clamping capacitors then:

$$m = k + 1 \tag{5}$$

$$l = 2(m-1) \tag{6}$$



(a)



(b)

Figure 5. The architecture of the FCMLI: (a) basic diagram; (b) simulation diagram used in Matlab Simulink.

$$N_c = \frac{(m-1)(m-2)}{2} \tag{7}$$

In this structure, the boot is more complex, because this topology has the disadvantage of requiring the precharge of the capacitors before beginning to operate as an inverter. However the stress on voltage switches is balanced with the number of levels, and it provides different combinations of switching states for the same output level.

To analyze this topology, only one phase will be taken in consideration. We used the diagram in **Figure 5(b)** on Matlab Simulink to study the 5 level FCMLI.

Figure 6 represents the output simulation results of the voltage, current, and voltage spectrum analyze successively. The simulation showed that the flying capacitor multilevel inverter that we used has an output voltage level THD of 35.34%. In the same power bank, and using the same load (R = 50 Ω, L = 100 mH), we have noticed a general power drop of 50.4 mv during a 1sec time simulation.

3.3. The Diode Clamped Multilevel Inverter (DCMLI)

This topology **Figure 7(a)** was first presented by [13] [14]; its main function is to use locking diodes to synthesize a sine wave from several voltage levels, typically obtained from capacitors that work as DC sources. The capacitors used are connected in series to divide the voltage.

If j is the number of clamping diodes per phase; we can find the following relations:

$$m = k + 1 \tag{8}$$

$$l = 2(m-1) \tag{9}$$

$$j = (m-1)(m-2) \tag{10}$$

In this structure the effort that each device must handle decreases as the number of levels increases. And yet interlocking diodes may handle the stress of more than one level. We used a single phase diagram to analyze this structure; the diagram **Figure 7(b)** was implemented on Matlab Simulink, Using the same command pattern as previously.

Figure 8 represents the output simulation results of the voltage, current, and voltage spectrum analyze successively. The simulation showed that the diode clamped multilevel inverter that we used has an output voltage level THD of 38.21%. In the same power bank, and using the same load (R = 50 Ω, L = 100 mH), we have noticed a general power drop of 12.3 mv during a 1sec time simulation.

3.4. The Cascaded H-Bridge Multilevel Inverter (CHMLI)

This topology [15] [16] performs the same function as the above, a sinusoidal voltage is generated from different DC sources; it is based on cascading full bridge inverters **Figure 9(a)**. This configuration is widely used in applications where the AC sources are destined to variable speed drives, and high voltage.

Each module may generate for itself different output voltage levels, 0, +V, or –V. By using different combinations we obtain the stepped AC voltage output. Generally if we consider Ns the number of independent DC sources per phase, then:

$$m = 2N_s + 1 \tag{11}$$

$$l = 2(m-1) \tag{12}$$

This converter can avoid the use of interlocking diodes or balancing capacitors. We can also get a low harmonic distortion by controlling the firing angles of different voltage levels. Furthermore this significant topology offers great flexibility to increase the number of levels. We used a single phase CHMLI to simulate the inverter; the diagram **Figure 9(b)** was implemented on Matlab Simulink.

Figure 10 represents the output simulation results of the voltage, current, and voltage spectrum analyze successively. The simulation showed that the diode clamped multilevel inverter that we used has an output voltage level THD of 35.12%. To simulate the impact of this inverter on the power bank, we divided it into two parts of 10 batteries each in a way that each section gives a 120 Vdc. We noticed that in the first section there is a general power drop of 58 mV while there is in the second section a power drop of 67 mV, during 1 sec time simulation.

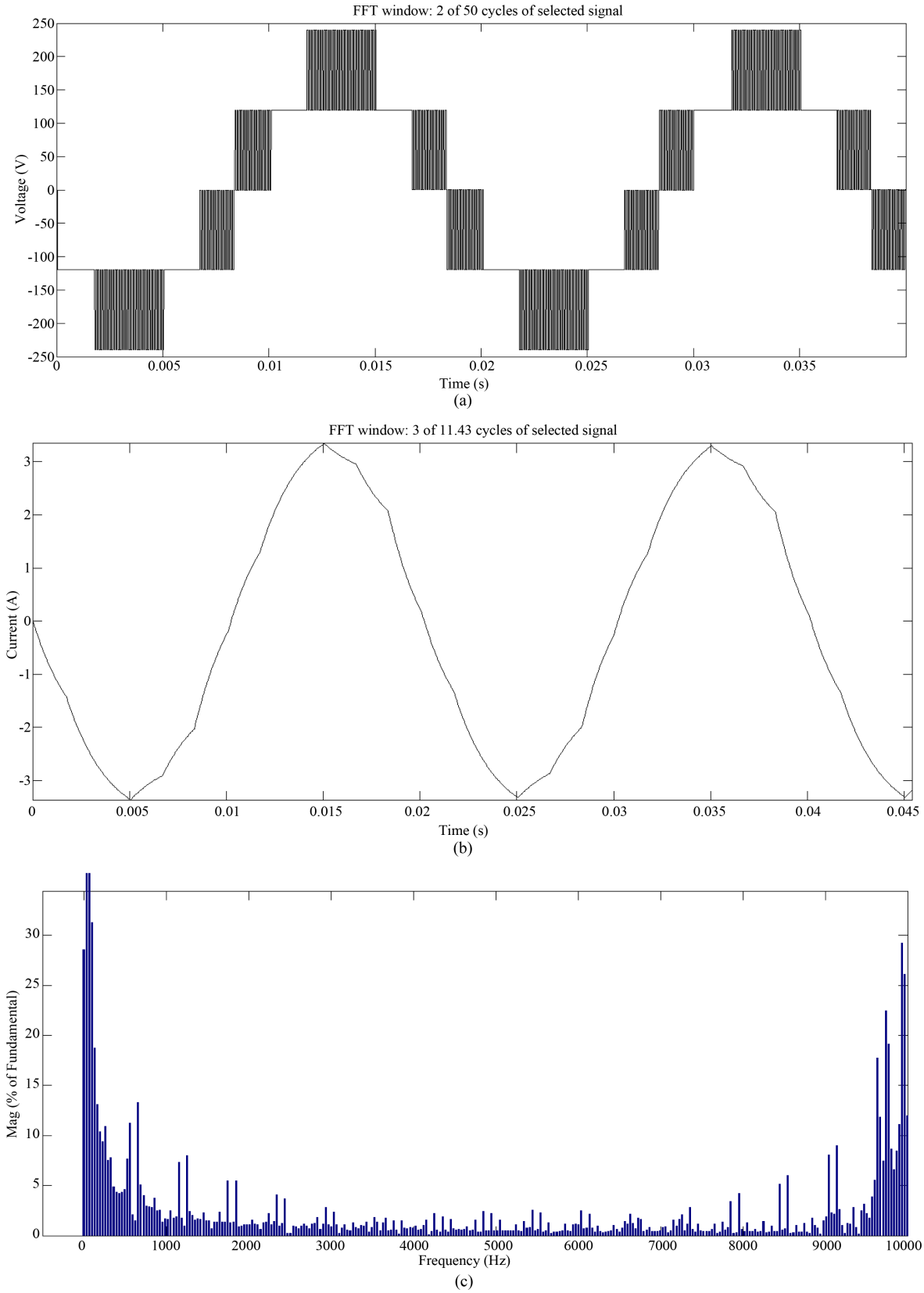


Figure 6. Output simulation results of the FCMLI: (a) voltage; (b) current; (c) output voltage spectrum analyze.

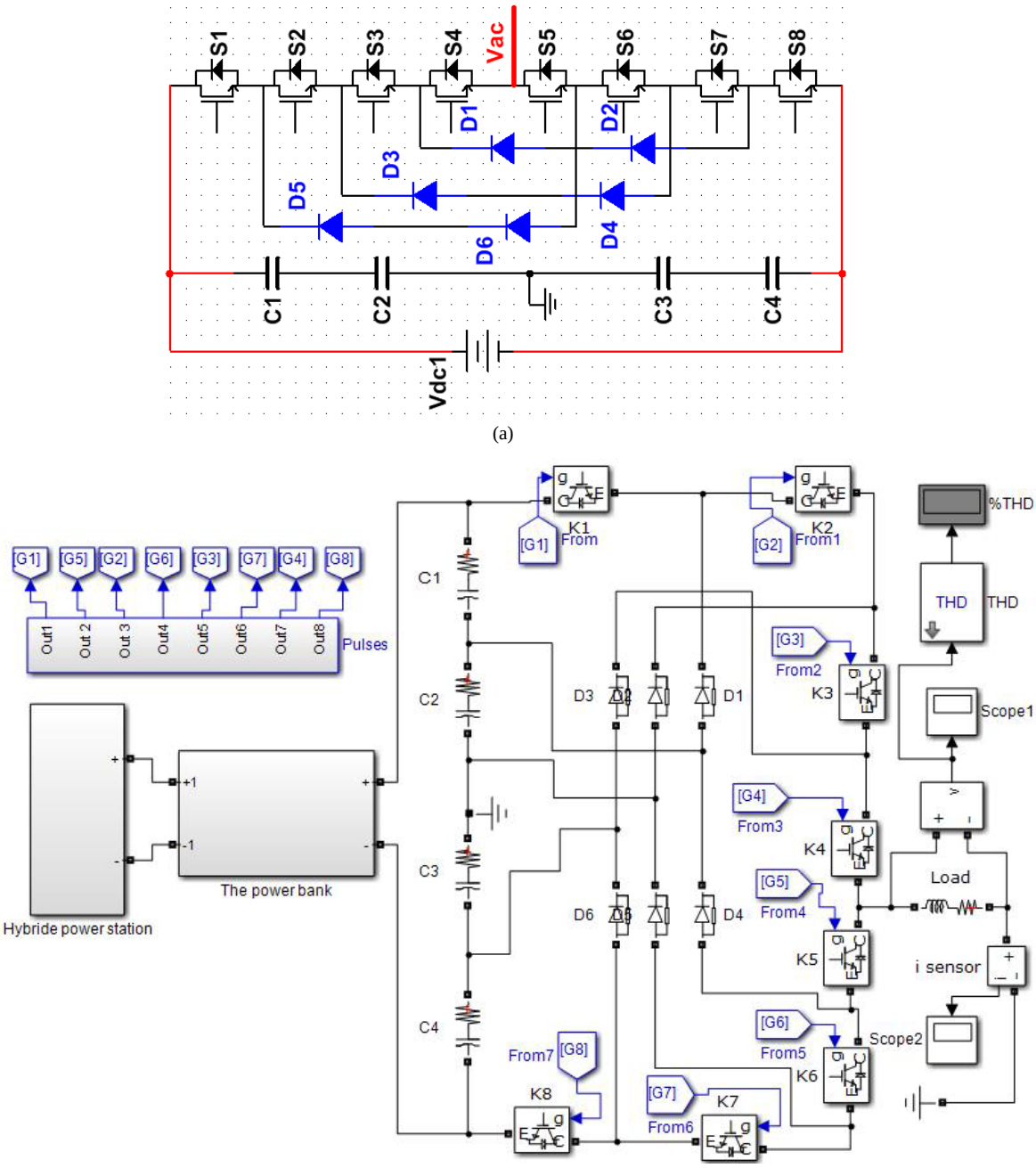


Figure 7. The architecture of the DCMLI: (a) basic diagram; (b) simulation diagram used in Matlab Simulink.

4. Effect of Level State on the CHMLI Performance

The CHMLI has shown the most promising features and performances, because it has the lowest THD in term of output voltage. Compared to the rest of multilevel inverters the cascaded H-bridge multilevel inverter requires the fewest number of components. CHMLI possesses a very importer characteristic; if we need to change the number of levels, this means increasing or decreasing the number of levels, there is no need to change the command laws, and there is no major change on the circuits, we only add or remove cells with a slight time shift on carriers. Thus we picked this inverter for more detailed testing. In attempt to establish the influence of the number of levels on the CHMLI performance, we simulated this multilevel inverter in different level states ranging from 5 to 15. **Table 1** summarizes all the simulation results obtained for the CHMLI from 5 to 15.

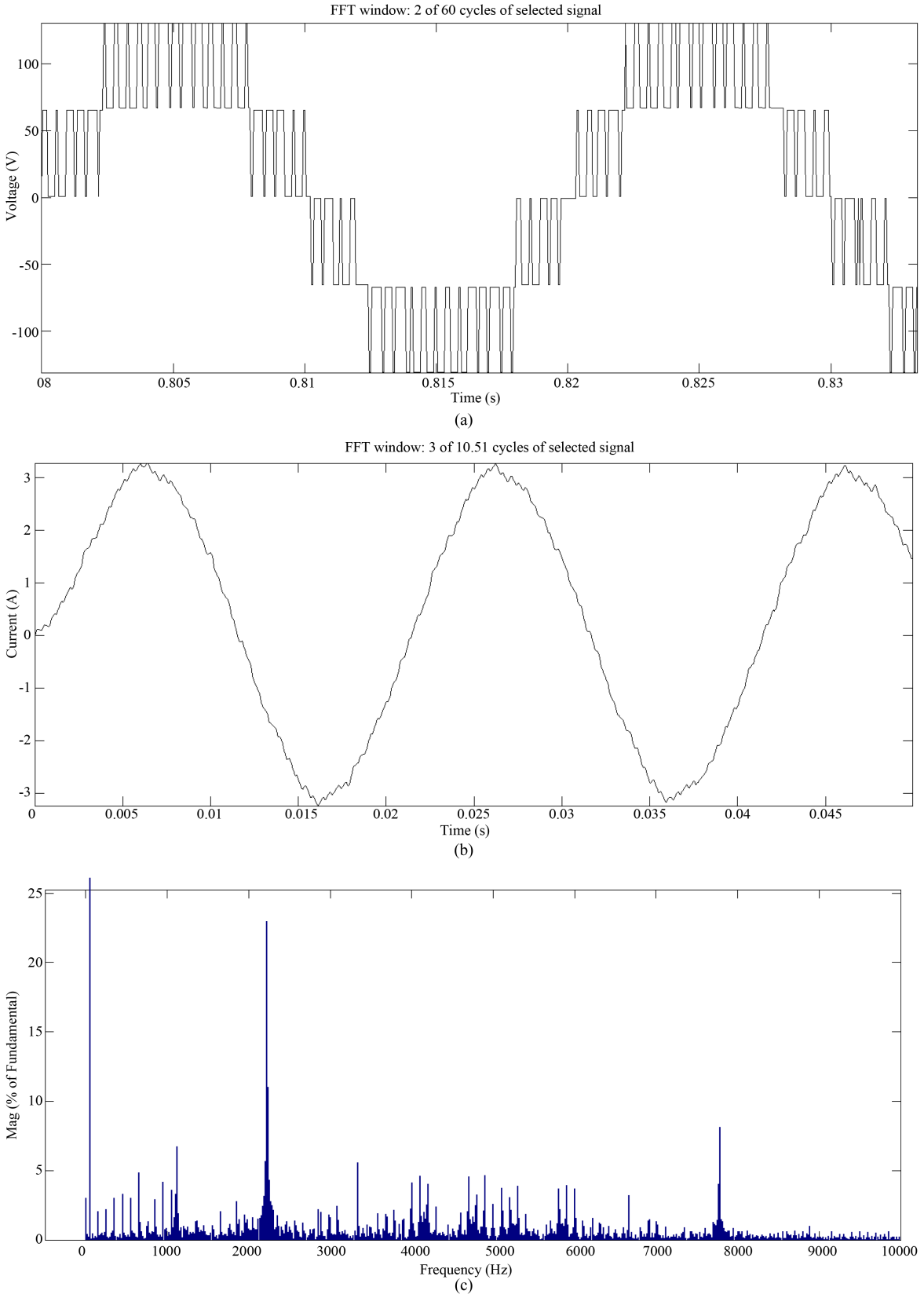


Figure 8. Output simulation results of the DCMLI: (a) voltage; (b) current; (c) output voltage spectrum analyze.

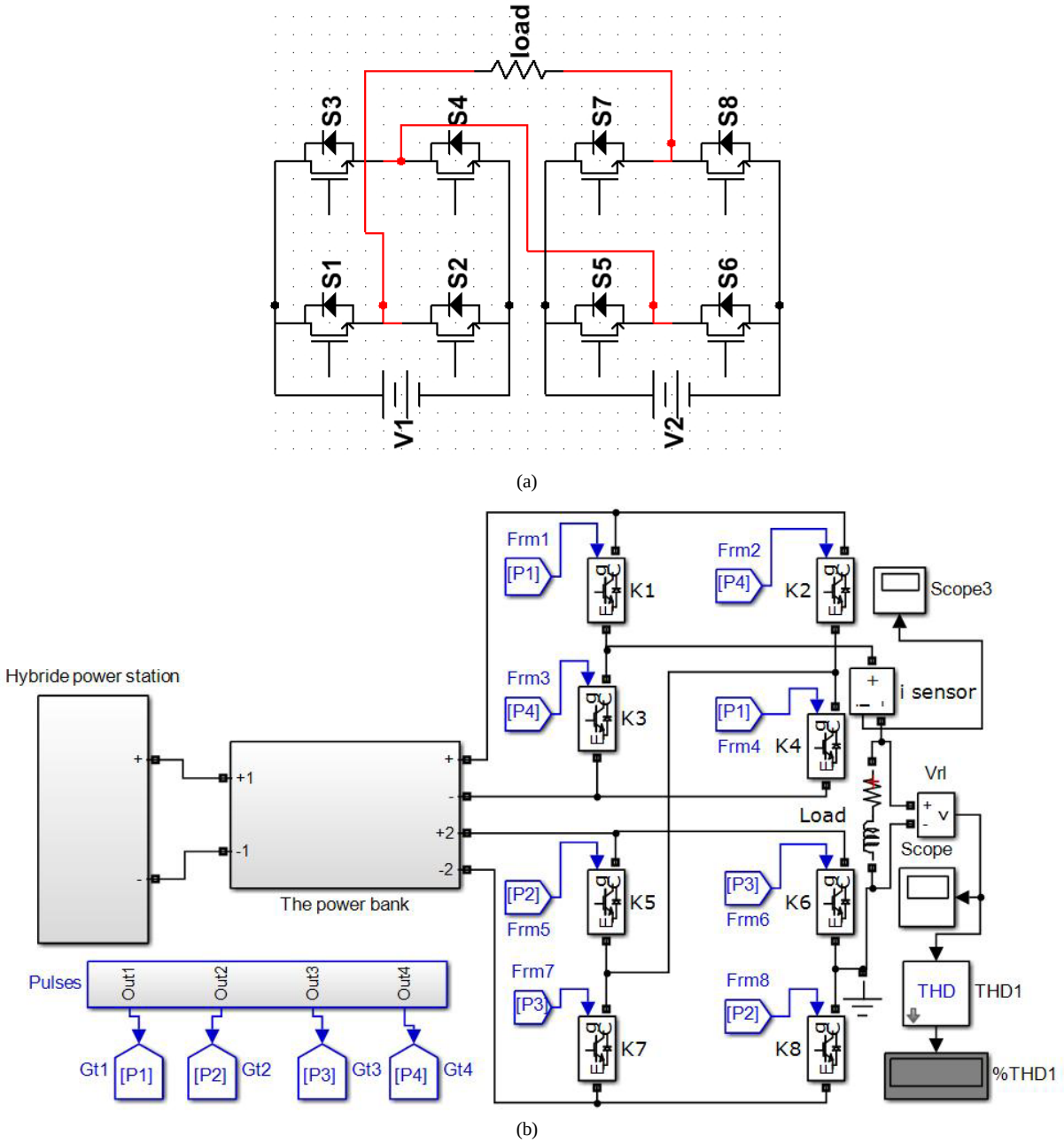


Figure 9. The architecture of the CHMLI: (a) basic diagram; (b) simulation diagram used in Matlab Simulink.

As it can be clearly observed in **Table 1**, starting from level 11, the THD decrease is slightly noticeable. The power drop is also more affecting. **Figure 11** represents the evolution of THD and power drop with the rising of levels.

As it can be observed in **Figure 11**, level 11 is the limit from where the THD's decrease is note very noticeable and the power drop is more important. Our primary objective is to choose the most efficient configuration of the CHMLI, which means getting a reasonable output current and voltage, yet at the same time the inverter has to be energy efficient. Therefore a CHMLI of more than 11 would not be a preferable investment for our hybrid renewable power station. Due to these conclusions we decided to aim our study toward the CHMLI with 11 levels in order to draw the most accurate results, **Figure 12** represents the diagram of the 11 levels CHMLI used in the study. We used the same simulative conditions as before in all the multilevel inverters concerned by this study.

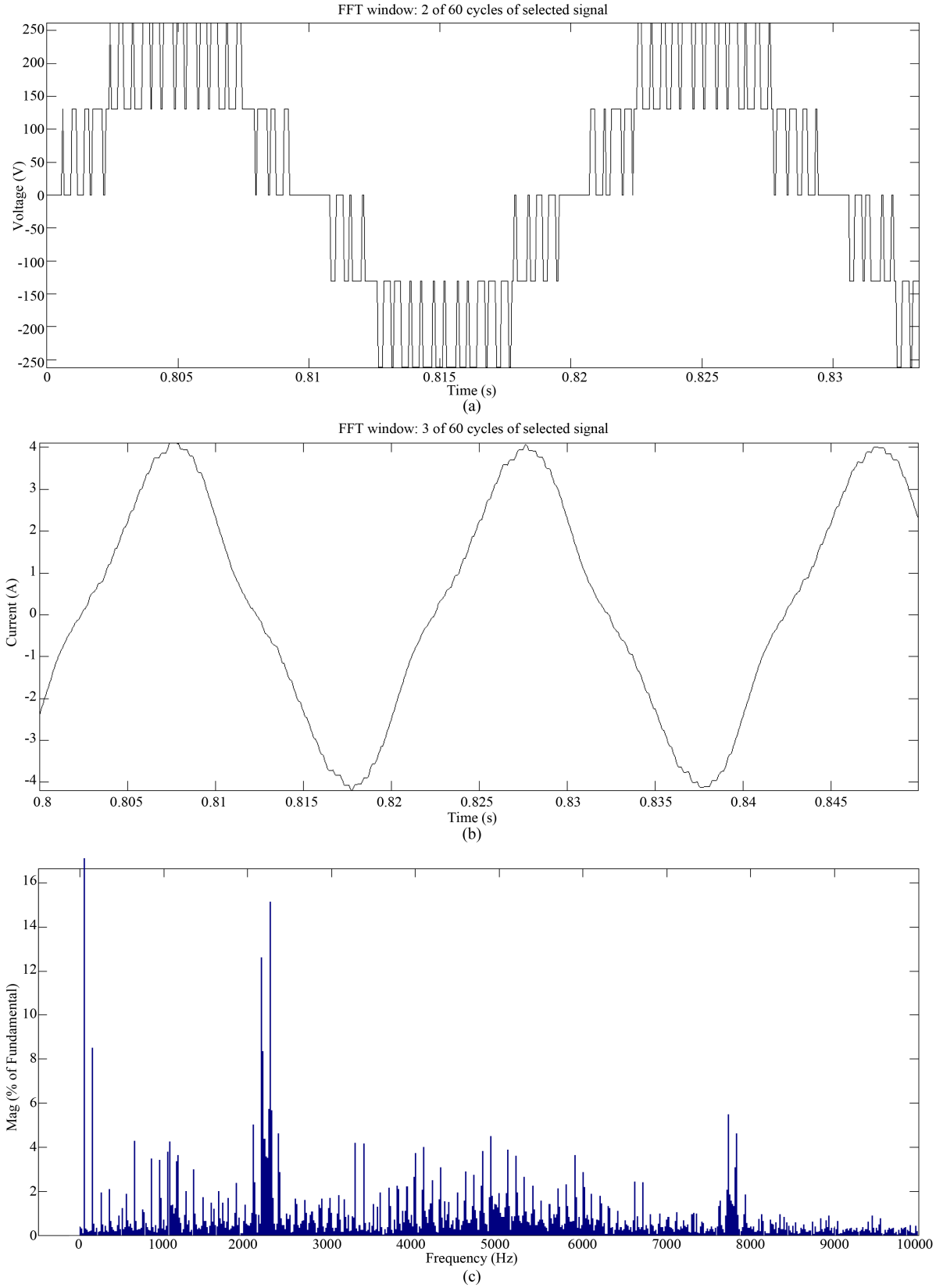


Figure 10. Output simulation results of the CHMLI: (a) voltage; (b) current; (c) output voltage spectrum analyze.

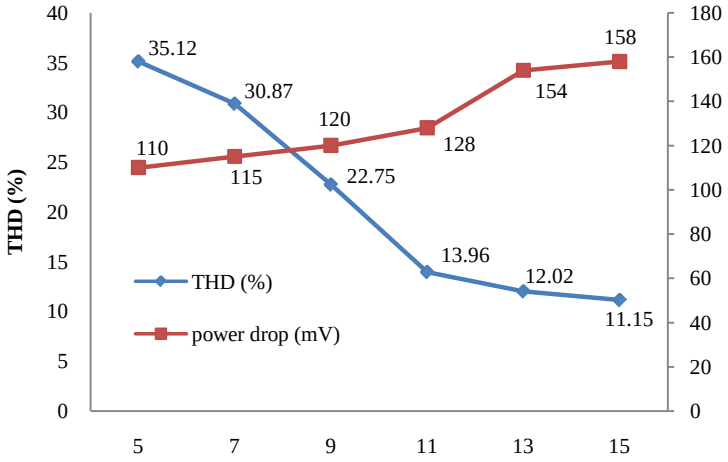


Figure 11. Simulation results of the CHMLI in many levels ranging from 5 to 15.

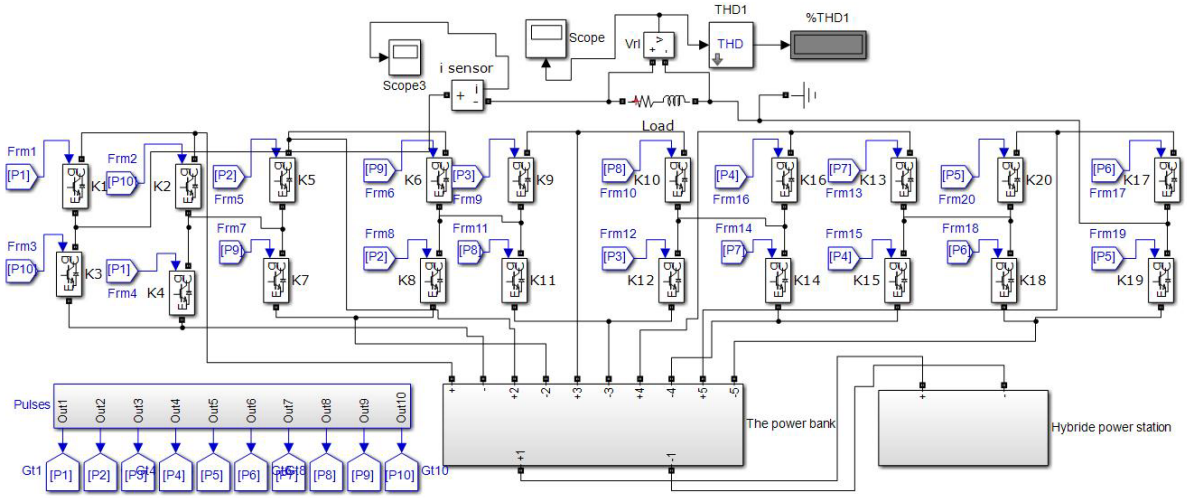


Figure 12. Diagram of the 11 levels CHMLI used on Matlab simulink.

Table 1. Simulation results of the CHMLI in many levels ranging from 5 to 15.

Level	Number of switching devices	THD (%)	Power drop (mV)
5	8	35.12	110
7	12	30.78	115
9	16	22.75	120
11	20	13.96	128
13	24	12.02	154
15	28	11.15	158

Figure 13 represents the output simulation results of the voltage, current, and voltage spectrum analyze successively. During the simulation of the CHMLI from level 5 to 15 we ensured that the previous simulation parameters were tightly respected, in order to have uniform results.

5. Discussion of the Simulation Results

In our study we found that the classic full bridge inverter has a THD of 76.51%. Despite its few components we

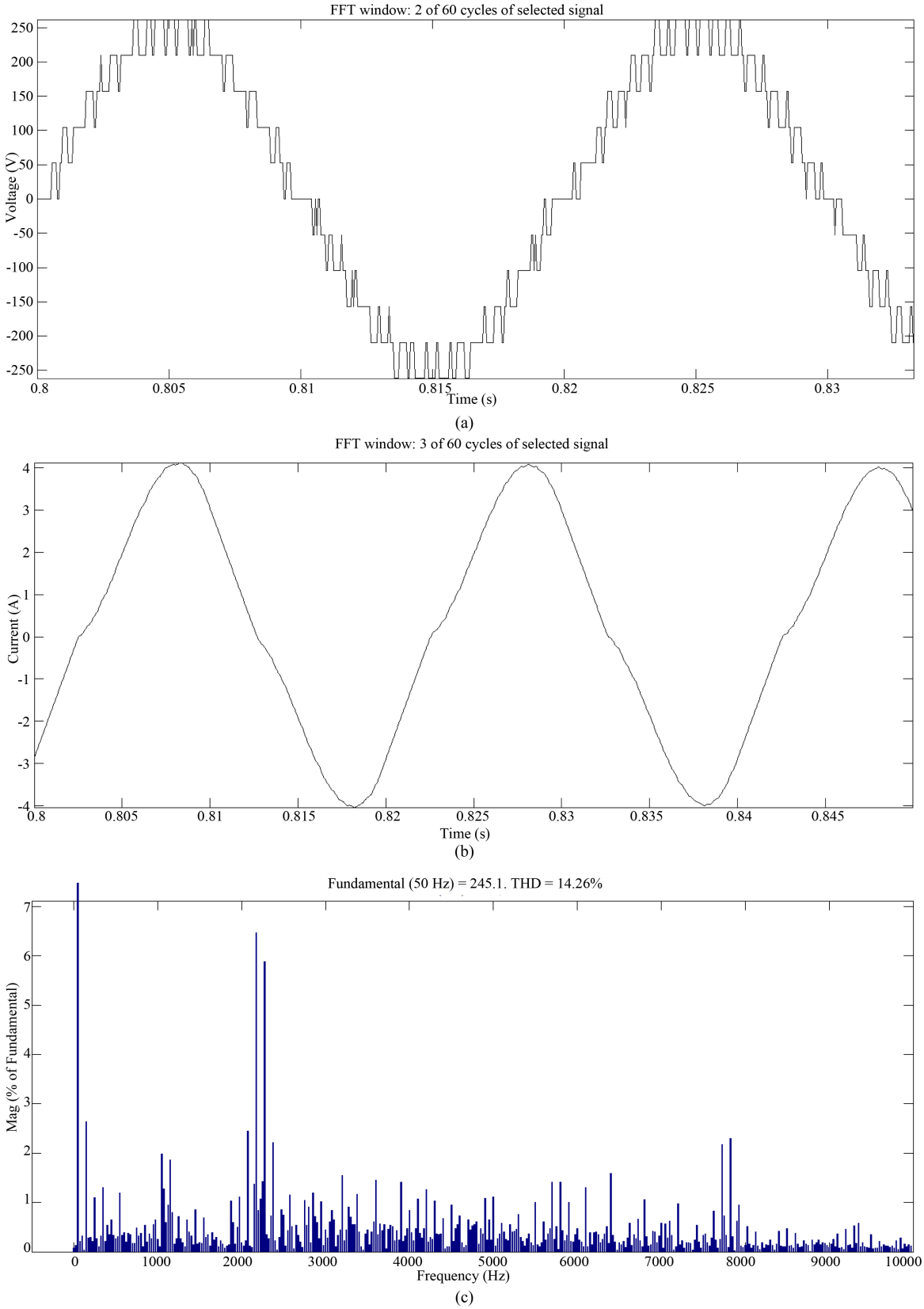


Figure 13. Output simulation results of the 11 levels CHMLI: (a) voltage; (b) current; (c) output voltage spectrum analyze.

noticed a 57.3 voltage decrease inside the power bank for the use of a (R = 50 Ω, L = 100 mH) load, during 1sec, which makes this inverter non effective for the use in the hybrid PowerStation.

The FCMLI circuitry, offers the advantage of providing extra switching combinations to balance the voltage levels, which may be used also to balance the switching losses, it also has a better signal quality (THD = 35.34%) than the DCMLI. But still the main default of the FCMLI is requiring excessive number of capacitors when the number of levels is high, which makes it difficult and expensive to implement. We noticed despite the components, the use of the FCMLI with a (R = 50 Ω, L = 100 mH) load causes a 50.4 mV general power decrease in the power bank.

We noticed in the DCMLI that it is possible to achieve a high efficiency. The use of filters can also be avoided when the number of levels is high enough. The simulation showed that the use of the DCMLI during a 1sec time, on a (R = 50 Ω, L = 100 mH) load causes a voltage drop in the power bank of approximately 12.3 mV; this allows us to say that the DCMLI has the lightest impact on the power bank. Despite these conclusions the DCMLI used still has a high THD (38.21%) compared to the rest of inverters. The DCMLI requires excessive locking diodes when the number of levels is high.

As it can be seen from the study, the CHMLI requires the fewest number of power components. thus to increase the number of levels, no diodes or capacitors are needed, each semiconductor switch manages a uniform stress, whatever is the level of the inverter, which makes it the easiest to implement. The 5 level CHMLI has also the lowest THD (35.12%); on the one hand this inverter needs separated DC sources, which can be used to divide the power bank in multiple sections, on the other hand the use of such inverter causes bigger voltage decrease in the power bank (58 mV in the first section, and 67 mV in the other one for a (R = 50 Ω, L = 100 mH) during 1 sec time simulation); this is normally due to the fact that the CHMLI is basically a cascaded set of full bridge inverters. Therefore we decided to raise the number of levels in an attempt to study the impact of level increasing upon the performance of the CHMLI. Thus the optimal level found was 11. In this level state the CHMLI in our study had a 13.96% THD, and caused a 128 mv power decrease inside the power bank during a 1 sec time simulation. On the basis of these conclusions we can affirm that the optimal choice for our hybrid power station is a CHMLI with 11 levels.

6. Conclusion

In our study a comparison was made between the three basic 5 levels inverters topologies: the FCMLI, the DCMLI, and the CHMLI using the a PWM law command, in order to draw accurate conclusions to develop the most adequate multilevel inverter for a hybrid wind-solar power station. In addition to the THD and the number of components this study reveals a unique comparison result on the impact of the multilevel inverter type on storage units. The CHMLI was identified as the most suited multilevel inverter for the hybride renwable power station, even if it causes a more important power drop. The FCMLI and the the DCMLI require both more components and have higher THD on the output voltage. This study has also shown unique findings related to the effect of level state on the efficiency of the CHMLI, in this countext we found that the CHMLI with 11 levels is the most efficient configuration for this type of multi level inverters. Furthermore we have found that impact on power storage units with level increasing for the CHMLI is less consistent compared to the signal purity obtained. These results pushes us to focus our effort on realizing an apropriate CHMLI for the renewable power station experimentaly speaking. In terms of perspectives a real time obtimisation command would allow us to get more sutisfying results witout altering the power consumption. Eliminating spesific harmonics is also a fast way to get a better power quality, but is still hard to implement in real time mode. Our prime goal is to get best performance by accomodation between real time optimization and harmonic elimination without compromising power storage eficiency.

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