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Performance Analysis and Technical Feasibility of an iUPQC in Industrial Grids

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Abstract

The iUPQC is a Unified Power Quality Conditioner in which the series converter emulates a sinusoidal current source and the shunt converter emulates a sinusoidal voltage source. This approach provides indirect power quality compensation of the load voltage and the source current. Recent studies have suggested that the iUPQC has technical advantages in comparison with the conventional UPQC due to its reduced switching frequency characteristic. In this paper, these technical advantages are investigated. Thus, the iUPQC performance is verified through a 150 kVA industrial equipment and technical design specifications are discussed: the iUPQC power circuit design, the converters arrangement and the driver configuration. Experimental results are provided to validate the technical feasibility and power quality compensation performance.

Keywords

Unified Power Quality Conditioner; iUPQC; Industrial Power Rate; Active Filter

1. Introduction

The Unified Power Quality Conditioner, UPQC, is a worthwhile equipment that provides power quality compensation since it is able to mitigate power quality issues of the utility current and of the load voltage, simultaneously. In this way, many studies have been focused on improving the UPQC effectiveness and robustness, as well as ensuring its viability in high power grids [1-4].

The viability aforementioned is mostly compromised by the converters switching performance because of the harmonic components synthesis for active filter compensations, reaching unviable switching losses in high power converters. Aiming to soften this weakness and provide faster dynamic performance, a dual topology of the conventional UPQC interchanges the source mimicked by the series and shunt converters [5-10], even though still using the same power-circuit configuration (**Figure 1**). This topology, named iUPQC or dual UPQC, controls the series converter as a sinusoidal current source and the shunt converter as a sinusoidal voltage source. Therefore, the harmonic components are mitigated without being handled by the iUPQC controller, improving its dynamic performance.

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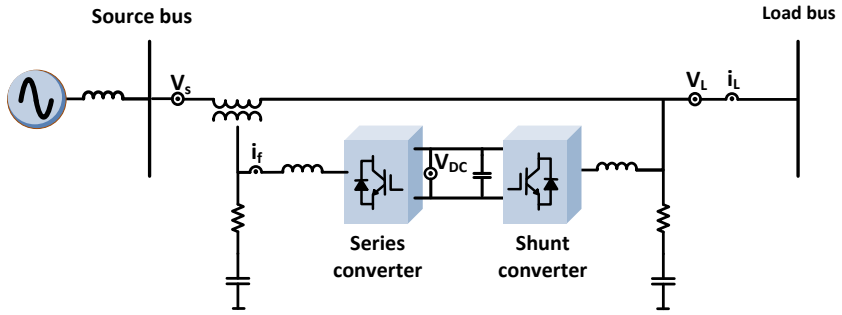

Figure 1. iUPQC Power circuit configuration.

In [8] the iUPQC performance was investigated using different switching frequencies. Experimental results from a laboratorial prototype have indicated that the iUPQC harmonic compensation is achieved even if a reduced switching frequency is employed. This suggested that the iUPQC is more appropriated than the conventional UPQC for power quality compensation in high power system, when a reduced switching frequency should be employed to obtain reduced switching losses and, consequently, reach its viability with the power converters currently available.

This paper carries out the iUPQC power quality compensation in an industrial power rate system. Thus, technical aspects are discussed according to the procedures performed to attain a 150 kVA iUPQC connection into the grid. In Section 2, the iUPQC power circuit design is discussed through the power flow analysis for proper dimensioning of the power components. The iUPQC commissioning tests are presented in Section 3 with the proper procedures to assure the power converters switching feasibility at nominal conditions. In Section 4, the provided experimental results present the transitory and steady-state iUPQC performances for the stated adjustments and nominal conditions.

2. iUPQC Power Circuit Design

The iUPQC power components are designed to allow the iUPQC operation with nominal load. Moreover, the steady-state active and reactive power flows in the aforementioned situation are used for dimensioning the power components appropriately.

The iUPQC used in this work is aimed to perform sag/swell voltage compensation up to 50% of the nominal voltage with full load (150 kVA). **Figure 2** depicts this situation. Moreover, this power quality issue associated with the nominal load connection provides the maximum steady-state overload situation of the iUPQC components. Therefore, this scenario provides a satisfactory condition for the iUPQC components design.

In a sag/swell source voltage disturbance, the iUPQC preserves the load bus voltage regulation and thus a voltage compensation (V_C) rises at the series coupling transformer. This voltage is a positive-sequence component at the fundamental frequency. According to the circuit, the voltage phasors of the positive-sequence component at fundamental frequency can be expressed as:

$$\dot{V}_L = \dot{V}_S + \dot{V}_C \tag{1}$$

Therefore, disregarding the system losses, the power flow in steady-state is:

$$S_{source} = P_{load} \tag{2}$$

$$Q_{shunt} = Q_{load} \tag{3}$$

$$Q_{source} = Q_{series} = 0\ VAr \tag{4}$$

$$P_{series} = P_{shunt} \tag{5}$$

where Equations (2)-(4) guarantee unit power factor at the source bus, and Equation (5) the power flow balance. The load current highlighted in **Figure 2** is due to the active power load consumption. In a sag/swell voltage disturbance, the V_C voltage and this load current cause an active power flow from the series converter to the system. Since Equation (5) must be satisfied in steady-state, this active power flows through the shunt converter, resulting in an internal circulating current (sag/swell current). Both currents (load and sag/swell currents) with

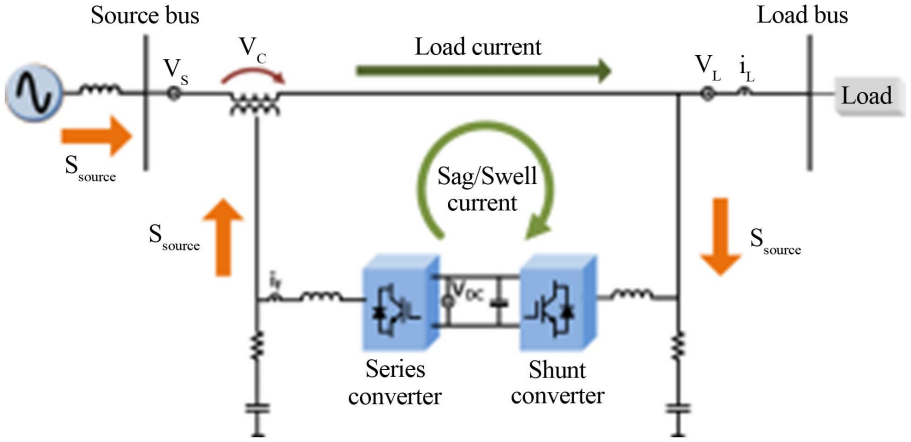

Figure 2. iUPQC with full load and 50% sag/swell compensation.

the highest amplitude in steady-state should be taken into account to the iUPQC components design.

For the branch between the source and the load buses, the highest current is achieved when only average active power is being consumed by the load further with the maximum sag/swell voltage disturbance. Thus, defining a constant ($k_{sag/swell}$) for the maximum allowable sag/swell voltage disturbance:

$$k_{sag/swell} = \left. \frac{\left|\dot{V}_{source}\right|}{\left|\dot{V}_N\right|} \right|_{\max\ sag/swell} \tag{6}$$

From (2):

$$\sqrt{3} \cdot k_{sag/swell} \cdot \left|\dot{V}_N\right| \cdot \left|\dot{I}_{source}\right| = \sqrt{3} \cdot \left|\dot{V}_N\right| \cdot \left|\dot{I}_{load}\right|$$

$$\left|\dot{I}_{source}\right| = \frac{\left|\dot{I}_{load}\right|}{k_{sag/swell}} = \left|\dot{I}_{load}\right| + \left|\dot{I}_{sag/swell}\right| \tag{7}$$

$$\left|\dot{I}_{sag/swell}\right| = \left|\dot{I}_{load}\left(\frac{1}{k_{sag/swell}} - 1\right)\right| \tag{8}$$

Therefore, Equation (8) indicates that the iUPQC components has to be designed to support currents in steady-state with amplitude values higher than the nominal load current amplitude, due to the voltage regulation of the load bus. It is important to highlight that high values will be achieved to sag voltage disturbances. Nevertheless, if the series converter is able to operate at higher voltage amplitudes, the coupling transformer can be useful to reduce the current in the series converter branch.

3. iUPQC Commissioning Tests

The industrial iUPQC parameters are shown in **Table 1**. These values were specified according to usual values of voltage, frequency and power rate in Brazilian industrial power grids. However, before connecting the iUPQC into the grid, commissioning tests were performed to certify the safe operation of the equipment in nominal conditions.

The commissioning tests are important to ensure safe conditions to the power converters switching. As a result, the switching devices parameters and frequency are established. The switching devices are composed by 6 drivers Semikron SKHI23 and 12 IGBT's SKM 400 GB 176 D with snubber $C = 0.22\ \mu F$.

Even though the switching devices are set according to the power rate, nominal voltage and switching frequency values, the power converter design as well the constructive arrangement of the equipment can cause unsafe operational conditions due to electromagnetic interference (EMI). The EMI are originated from the IGBT switching and are also produced by high dv/dt output voltages and/or inductive load current switching [11-13].

Table 1. iUPQC parameters.

Parameter	Value
Voltage	440 V rms
Grid frequency	60 Hz
Power rate	150 kVA
DC-link voltage	850 V dc
DC-link capacitors	C = 36267 µF
Shunt converter passive filter	L = 170.0 µH R = 1.0 Ω C = 300.0 µF
Series converter passive filter	L = 340.0 µH R = 2.0 Ω C = 150.0 µF
Sampling frequency	5130.0 Hz

Moreover, the EMI may adversely affect the driver operation. In order to mitigate the EMI, **Figure 3** depicts the converters arrangement, where the drivers are placed just in the back-side of the IGBT connection buses. This should reduce the EMI in the drivers due to the electromagnetic isolation provided by the metallic sheet between the drivers and the IGBT busses, and also due to the resultant short cables that connect the drivers to the IGBTs.

In the commissioning tests, the first approach set the driver components at the following values: $RG_{on} = RG_{off} = 6.8\Omega$, $R_{ce} = 18k\Omega$, $C_{ce} = 430\,pF$ and dead time $t_{td} = 5\,\mu s$. According to the driver datasheet, these values may be adjusted to avoid additional losses or even the destruction of the IGBT. Hence, the commissioning test was accomplished as shown in **Figure 4**, in order to obtain reduced collector emitter voltage (V_{ce}) spike with appropriated switching frequency and dead time.

The commissioning test procedure is performed by increasing the ac voltage (V_{ac}) and current (I_{ac}) through the PWM control and the variable load, respectively. The dc voltage (V_{dc}) was regulated to 700V. Then, the V_{ce} voltage was verified in order to obtain acceptable spike values, according to the IGBT datasheet. For the first approach values, **Figure 5** depicts the V_{ce} voltage when $V_{ac} = 219.5$ V and $I_{ac} = 103.7$ A. The spike voltage reached unacceptable values (about 2.5 KV).

The second approach increased the resistances values to $RG_{on} = RG_{off} = 12.0\Omega$. This is the recommended driver datasheet procedure to fit to the equipment application. As depicted in **Figure 6**, acceptable spike values were achieved with $V_{ac} = 296.3\,V$ and $I_{ac} = 131.1\,A$.

The results obtained through RG_{on} and RG_{off} adjustments guarantee the iUPQC safe operation with a switching frequency of 5130.0 Hz and dead-time of 5 µs. As the iUPQC converters synthesize sinusoidal references, these frequency and dead-time values should be enough to allow the active filter capability.

4. Experimental Results and Design Changes

After successful accomplish commissioning tests in the series and shunt converters, the iUPQC is ready to be connected to the system. Nevertheless, a design change in the shunt converter passive filter configuration can bring additional benefits in the equipment performance.

In this way, the arrangement of the passive filter of the shunt converter was modified with the RC branch connected at the load bus, instead of the conventional connection displayed in **Figure 1**, where it is connected together with the passive filter inductor. This change allows the RC branch current measurement by the i_L current sensor. In other words, the RC branch current is measured as the branch was a load and thus this current will be also compensated by the iUPQC.

The harmonic current compensation was verified through the iUPQC performance with a three-phase full bridge diode rectifier. **Figure 7** shows the steady-state harmonic compensation and **Figure 8** shows the transitory response through the load connection. Despite the reduced switching frequency due operational requirement

Figure 3. Converters arrangement; (a) detail of the IGBT buses and (b) Driver placed in the converter back-side.

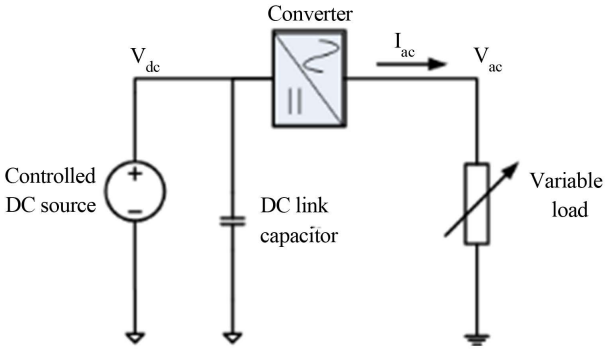

Figure 4. Commissioning test.

(5130.0 Hz) the harmonic current THD was reduced from approximately 25% at the load bus to 7.5% at the source bus. Moreover, the iUPQC achieve fast dynamic response, reaching the steady-state with sinusoidal waveform in approximately 4 cycle's period. These favorable results can be attributed to the iUPQC control strategy, which does not synthesize the harmonic components to compensate them.

For a two-phase load connection, the iUPQC controller has to synthesize sinusoidal three-phase currents at the series converter. In this manner, this three-phase current will supply the average active power of the load and the unbalanced current will be supplied by the shunt converter. **Figures 9** and **10** depict the experimental results of a two-phase full bridge diode rectifier connected at the load bus with the three-phase current drawn at the source bus. It is important to highlight that the source currents are three-phase sinusoidal currents with reduced harmonic and unbalanced components, in spite of the unbalanced two-phase harmonic load currents drawn at the load bus (two-phase diode rectifier).

Figure 11 depicts the voltage regulation in steady-state with the two-phase load aforementioned. The rms-

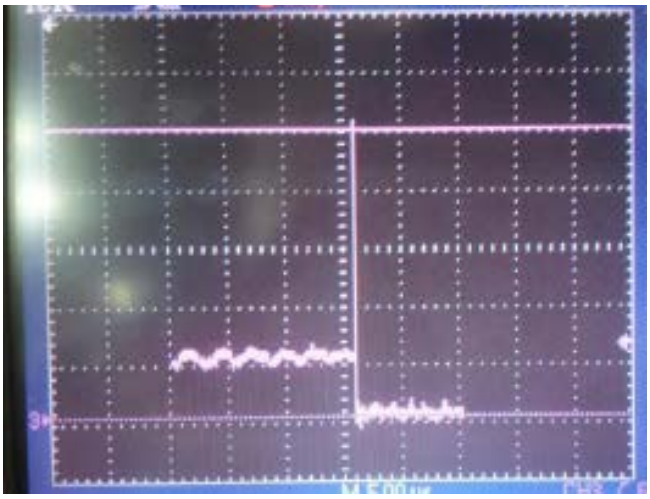

Figure 5. IGBT collector emitter voltage. 5 μs/div, 500 V/div.

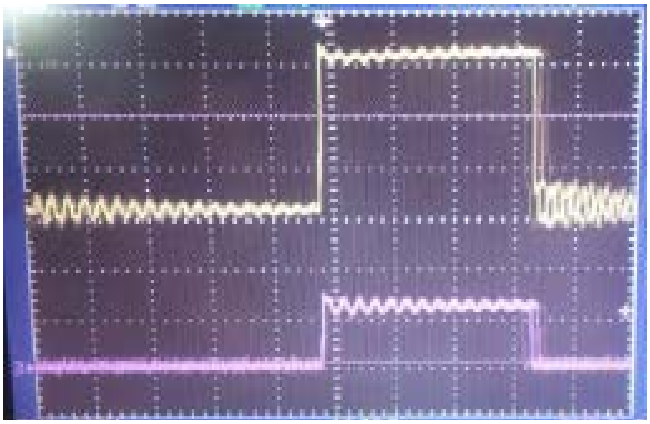

Figure 6. IGBTs collector emitter voltage. 5 μs/div, top signal 500 V/div and bottom signal 500 V/div.

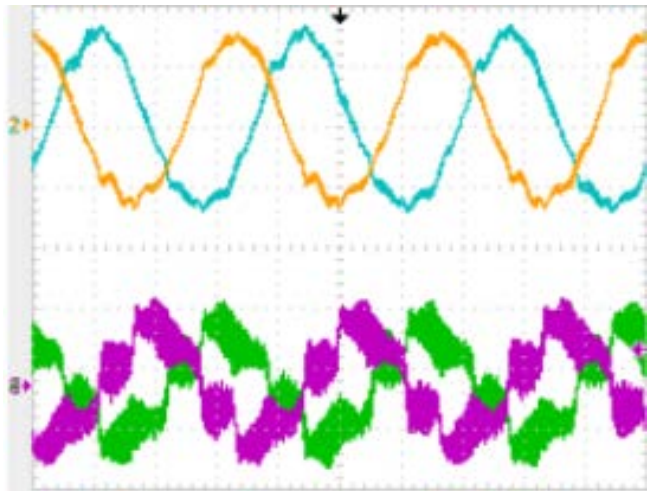

Figure 7. Source current compensation in steady-state with three-phase full bridge diode rectifier; load currents (pink and green) and com-pensated source currents (yellow and blue); 5 ms/div, 100 A/div.

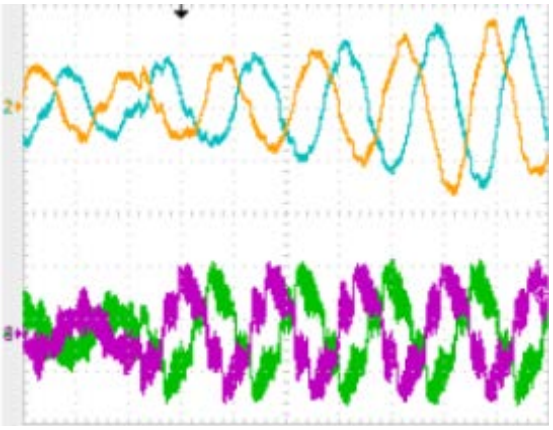

Figure 8. Source current compensation in transitory load connection with three-phase full bridge diode rectifier; load currents (pink and green) and compensated source currents (yellow and blue); 5 ms/div, 100 A/div.

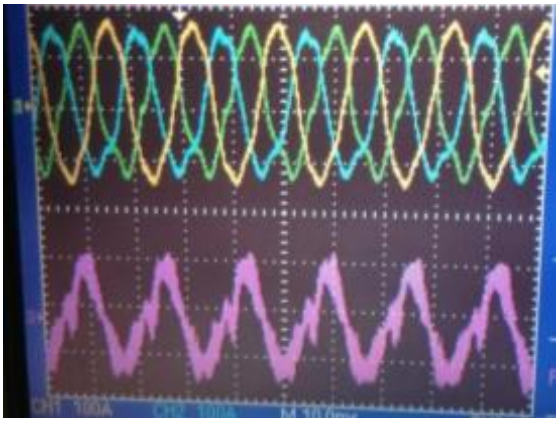

Figure 9. Source current compensation in steady-state with two-phase full bridge diode rectifier; load current (pink) and three-phase compensated source currents (yellow, blue and green); 5 ms/div, 100 A/div.

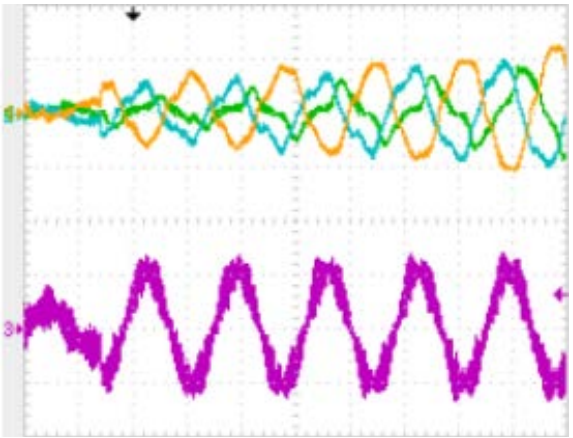

Figure 10. Source current compensation in transitory load connection with two-phase full bridge diode rectifier; load current (pink) and three-phase compensated source currents (yellow, blue and green); 5 ms/div, 100 A/div.

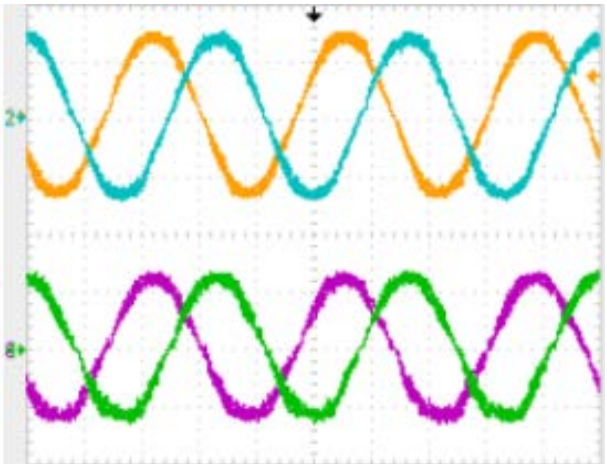

Figure 11. Load voltage regulation in steady-state with two-phase full bridge diode rectifier; source voltage (yellow and blue) and compensated load voltages (pink and green); 5 ms/div, 500 V/div.

load voltage was regulated around the nominal value even with a swell voltage disturbance at the source bus. Moreover, the voltage unbalance at the load bus was retained in acceptable values in face of the unbalanced load.

5. Conclusions

The iUPQC design specifications were discussed to an industrial power rate equipment. In this way, the components design can be obtained through the equipment power rate, the maximum sag/swell voltage regulation capability and the nominal power load consumption.

Commissioning tests were used in order to verify the iUPQC operation viability due to the collector emitter voltage spikes which could damage the converters switching devices. In addition to the proper configuration of the driver components, the commissioning tests are also useful to determine the allowable maximum switching frequency and minimum dead-time of the IGBTs.

The iUPQC performance was verified after the commissioning tests adjustments. Thus, despite the reduced switching frequency adopted, the iUPQC performance guarantees the harmonic source current mitigation and the load voltage regulation with balanced and unbalanced harmonic loads.

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