**Design and Implementation of a Novel Digital Frequency Superposition Testing Power Supply for Induction Motor**

Xingjian Dong¹, Shenxian Zhuang¹, Wen Yan²

¹School of Electric Engineering, Southwest Jiaotong University, Chengdu, China; ²Hunan YinHe Electric Corporation, Changsha, China.
Email: swjtu_dxj@126.com

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**ABSTRACT**

A novel design and implementation of frequency superposition testing power supply for induction motor is proposed. An equivalent power using dynamic space voltage vector synthesis is generated to replace the two separate powers of the traditional method. The principle of frequency superposition testing is firstly introduced, and then the detailed design and implementation of the digital frequency superposition power are given. The simulation of the power supply system shows the promising results. Finally, experimental results validate the feasibility and reliability of the proposed power.

**Keywords:** Digital Power, Frequency-Superposition Testing, SVPWM

1. **Introduction**

Currently, there are two main methods for temperature rising testing which is an important index of induction motors. One is direct loading testing; the other is frequency superposition testing [1]. When a direct loading testing is performed, a duplicate motor must be coupled with the tested induction motor mechanically. However, for a large scale induction motor, it’s difficult to add a rated load on the shaft and it’s not safe. Frequency superposition testing is an equivalent loading testing without a duplicate motor coupled. The tested induction motor is fed with two separate voltage sources of two different frequencies. When a frequency superposition testing is performed, the most sophisticated case is that the two power supplies are supported by a dynamotor. There must be at least 4 to 5 operators to operate it. Another drawback is that the dynamotor runs with a big noise.

This paper designs and implements a digital frequency superposition testing power supply by using open loop constant volts per hertz control based on SVPWM (Space Vector Pulse Width Modulation). The reference voltage is synthesized with the main reference voltage and the auxiliary reference target voltage by using parallelogram rule. The two reference voltages are controlled via a HMI (Human Machine Interface) client.

The concept of frequency superposition testing is simply described in Section 2. The method to generate a synthesized voltage vector using space voltage vector synthesis and the digital implementation of the frequency superposition testing power supply are described in Section 3. The simulation and the experiment results of the power supply proposed are given in Section 4, Section 5 respectively. The conclusion is presented in Section 6.

2. **Traditional Frequency Superposition Testing Power**

In the traditional frequency superposition testing [1,2], the tested motor is fed with two independent powers coupled with a transformer. Figure 1 shows the schematic of the traditional frequency superposition power with dynamotor fed. Traditionally, the auxiliary frequency is (80% - 120%) times of main frequency. Under the synthesized power supply, the voltage, current, speed, flux of the tested motor run with a beating frequency. When the synthesized stator flux runs faster than the rotor’s, the tested motor runs as a motor, when the synthesized stator flux runs slower than the rotor’s, the tested motor runs as a generator. The RMS (Root Mean Square) values of the stator currents increase while the auxiliary voltage increases. Until the RMS values of the electrical parameters are around the rated values. The motor works as a rated load added on its shaft.
Design and Implementation of a Novel Digital Frequency Superposition Testing Power Supply for Induction Motor


3.1 Design of the Proposed Frequency Superposition Testing Power Supply

The hardware diagram of the proposed power has been shown in Figure 2. The hardware system consists of 1 power converter unit, 1 digital control board, 1 power analyzers and 1 HMI client.

The drive is based on TMS320LF2812 DSP platform. The main and auxiliary reference voltages are sent to the control board from the HMI client.

3.2 Implementation of the Power Converter Unit

The structure of the proposed three-phase voltage source power converter is shown in Figure 3. Uu, Uv and Uw are the output voltages. S1...S6 are the six IGBTs that shape the output, which are controlled by Su+ and Su-, Sv+ and Sv-, Sw+ and Sw-. When an upper IGBT is switched on, the corresponding lower IGBT is switched off, i.e., when Su+, Sv+ or Sw+ is 1, the corresponding Su-, Sv- or Sw- is 0. The on and off demonstrates the states of the up transistors S1, S3 and S5.

There are eight possible combinations of on and off patterns for Su+, Sv+, Sw+. The derived output phase and line-to-line voltages in terms of DC supply voltage Udc are shown in Table 1.

The objective of SVPWM technique [3] is to approximate the reference voltage vector Uo by a combination of the eight switching patterns. One combination is shown in Figure 4.

For every PWM period, the desired reference voltage Uo can be approximated by having the power converter in two adjacent switching pattern Ux,Ux+1 of T1 and T2 duration, respectively. The output voltages are decided by the selection of the duration time T1 and T2. The output voltage space vector is shown in Figure 5.

3.3 Synthesis of the Output Reference Voltage

Figure 6 shows a synthesis of the dynamic space voltage vectors.

According to Figure 6, using the parallelogram rule, we have:

\[ U_{\text{out}} = \sqrt{U_{\text{main}}^2 + U_{\text{aux}}^2 + 2 U_{\text{main}} U_{\text{aux}} \cos(\alpha_2 - \alpha_1)} \]

\[ \alpha = \arg \left( \frac{U_{\text{main}} \sin \alpha_1 + U_{\text{aux}} \sin \alpha_2}{U_{\text{main}} \cos \alpha_1 + U_{\text{aux}} \cos \alpha_2} \right) \]

where, \( U_{\text{main}}, \alpha_1 \) are the amplitude and electrical angle of the main voltage vector. \( U_{\text{aux}}, \alpha_2 \) are the amplitude and electrical angle of the auxiliary voltage vector. \( U_{\text{out}}, \alpha \) are the amplitude and electrical angle of the synthesized voltage vector.

Figure 2. Hardware diagram of digital power for frequency superposition testing
5. Experimental Results

Figure 8 shows the DC bus voltage and the stator current obtained with the Tektronix Scope. Such experimental results were obtained with a roller induction motor. The parameters of the tested motor the experiment are given in Table 2.

In this case, the main frequency is given to 21.8Hz, the auxiliary one is 17.8Hz (82% of 21.8). The auxiliary voltage is 0.2 times as the main power which is given to the rated voltage.

This experimental figure shows that the stator current is oscillated at a RMS value equals to the rate current.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated voltage (V)</td>
<td>380</td>
</tr>
<tr>
<td>Rated current (A)</td>
<td>107</td>
</tr>
<tr>
<td>Rated frequency (Hz)</td>
<td>21.8</td>
</tr>
<tr>
<td>Rated power (kW)</td>
<td>60</td>
</tr>
</tbody>
</table>
Design and Implementation of a Novel Digital Frequency Superposition Testing Power Supply for Induction Motor

Figure 7. Simulation results of the stator phase A current and the DC bus voltage

Figure 8. Experimental results of the proposed frequency superposition power supply

6. Conclusions

In this paper, a design of digital motor drive for frequency superposition testing is proposed. It has been implemented in an open loop control by using digital signal processor TMS320LF2812. Simulation results show that the stator current oscillated at a beating frequency after Frequency-Superposition. The tested motor runs as a rated load coupled with it. The experimental results indicate that this power supply can realize the equivalent loading test.

REFERENCES