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Research on Parallel Interleaved Inverters with Discontinuous Space-Vector Modulation*

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ABSTRACT

Parallel converter can significantly increase the capacity of the converter and improve the power quality of AC side, but the circulation which can lead to high switching loss and even damage the devices will easily exist in the direct parallel converters. In this paper, the average model of parallel interleaved inverters system to analyze the circulation current is shown, and the cross current is relevant to DC-bus voltage and the overlap time of zero vectors in the switching period. Based on this observation, a discontinuous space vector modulation without using zero vectors (000) is eliminate and suppress the zero-sequence current to entire system. Finally, the effectiveness of modulation strategy is verified by the simulations in this paper.

Keywords: Interleaved Inverters; Circulating Current; Discontinuous Space-vector Modulation; Zero- sequence Current

1. Introduction

With the increasing demand for power equipment capacity and quality, how to improve the capacity of the power electronic converters and improve its output performance is an important development direction of modern power electronics technology. High-frequency inverters due to the switching frequency and the power devices loss limit, the single component of the inverter only suitable for low or medium capacity occasions. In recent years, in the application of high power applications, the multi-level, mixed topologies, or parallel multiple methods is an effective way for expansion of the capacity of the inverters.

Three-phase inverter parallel system has many advantages, such as the system can achieve high current level, the current and voltage ripple is small, the parallel system has higher bandwidth. Previous research on parallel systems are mainly concentrated in the UPS, motor drives, as well as to improve the power factor occasions [1-2,4-6]. With the development of IGBT and other power semiconductor device of intelligent control to the integrated structure, now more and more application modules are directly connected in parallel, especially where a high power density integration is required, such as power sources, traction systems, uninterruptible power supplies, power factor correction circuits and active power filters (APF), and high power photovoltaic power generation system [3,8], through parallel technology to improve converter power and current levels, and enhance the redundancy of the system. therefore, parallel PWM inverter technology is of great significance for the promotion of high-power photovoltaic, wind power applications。

Putting modules in parallel, however, is not risk free. One of the major concerns for the parallel operation of a three-phase system is the cross-coupling between the three-phase system parallel modules, i.e., when each module in a certain switching state, the inverter module is connected with a DC bus at the same time to a common power supply or load, to increase the system does not require the circulation loop. In order to avoid this problem, the traditional method is to use an isolation transformer [4-5]. However, the use of transformer will undoubtedly increase the size and cost of the inverter system, especially in the high power and low switching frequency occasions, this problem more prominent. Therefore, the power converter modules are directly connected in parallel is required[3].

Through a comprehensive system analysis using the averaged model, this paper shows the mechanism of how the zero-sequence current is produced with the interleaved technology, and the peak of zero-sequence current is related to DC voltage and the overlap time of zero vectors in a switching period. The discontinuous space

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vector modulation without using zero vectors is used to eliminate the cause of pure zero-sequence current for parallel operation. Simulation results are discussed which are obtained to validate the theoretical analysis.

2. The Principle of Interleaved Modulation

2.1. General Description

The system to be analyzed is shown in **Figure 1**.

It is composed of two three-phase inverters connected in parallel. Each phase(A, B, C) is composed of two commutation cells (a and b) which DC input side directly connected to the DC bus , and AC side output connected to the grid through inductors.

The interleaved modulation of two inverter modules is shown in **Figure 2**, module 1 and module 2 using the same three-phase sine-wave voltage as a modulated wave, and the carrier phase shift 180^0, each phase has the same fundamental wave. When the switching frequency is high enough (and the Carrier ratio is large), the three-phase modulated wave can be regarded as a DC constant in a switching period, the driving waveform of right bridge in phase A can be regarded as a half shift in carrier cycle to the left bridge. The driving waveform of two modules can be obtained from **Figrue 2** [1].

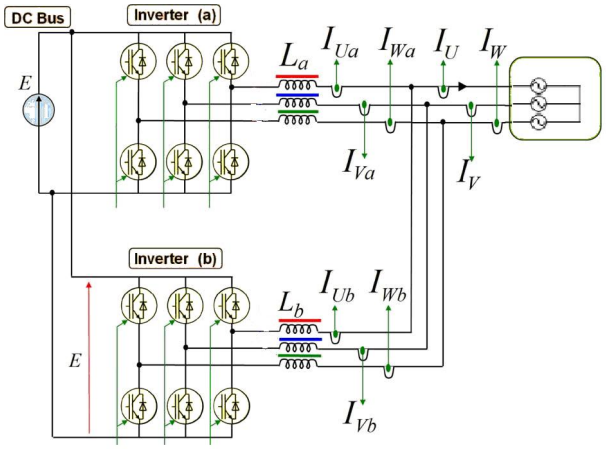

Figure 1. Typical configurations of interleaved inverters.

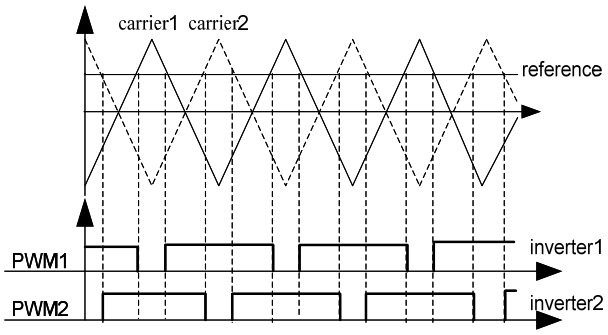

Figure 2. The principle of interleaved modulation.

We take the phase A as an example, a simplified diagram is shown in **Figure 3**.

Ua1 and Ua2 are the voltage of phase A between the two interleaved inverter modules, two inverters will transmit power to the grid together, at the same time as Ua1, Ua2 and inductance L has a circulation path, when the two inverters output voltage Ua1 and Ua2 are inconsistent or the two inverter parameters is inconsistent, it will produce cross-current, when the two inverters output voltage Ua_1 and Ua_2 are inconsistent or the two inverter parameters are inconsistent, the crossing current is I_H. We assumed that the parameters of the two inverters is completely consistent, from **Figure 3** we can obtain the output voltage Uao of the interleaved inverter [2,3].

$$U_{ao}=(U_{a1}+U_{a2})/2 \quad (1)$$

Even two modules of the system parameters, dead-time entirely consistent, due to the interleaved modulation, it will also cause the two inverter output voltage instantaneous value are inconsistent, the difference voltage in the same phase between the output voltages of the two inverter modules are inherent[8,9], the differential mode component will be the formation of crossing current I_H

$$I_H=(U_{a1}-U_{a2})/2X_L \quad (2)$$

2.2. Analysis of the Circulating Current

With interleaved parallel technology, it can greatly reduce the output current ripple of high-frequency inverter [1-3,6]. In high-power applications, using interleaved parallel technology, the single tubes resistance can be reduced by half, in the same current ripple requirement, the size of the inductor can be greatly reduced, and the dynamic response of the entire system can be improved accordingly[3,7]. However, since the inverter is directly connected in parallel, in addition to the common mode component power supply for load or grid, while the two interleaved parallel modules generate the differential mode component, and this component will flow between the two modules, this is circulation current, the circulation current performance for zero-sequence component, inhibit the Zero Sequence circulation current is conducive to improve the current stress of the inverter module switchs.

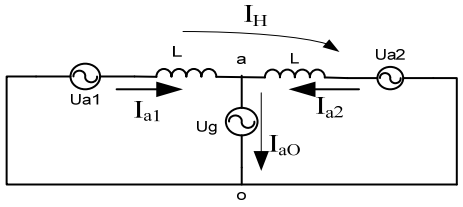

Figure 3. The simplified diagram of two interleaved inverters.

For zero-sequence current of the parallel three-phase inverter can be expressed as

$$i_{h0}=(i_{La1}+i_{Lb1}+i_{Lc1})/3=-(i_{La2}+i_{Lb2}+i_{Lc2})/3 \quad (3)$$

At any time the switching state function can be obtain as:

$$S_1=(S_{a1}+S_{b1}+S_{c1})/3$$

$$S_2=(S_{a2}+S_{b2}+S_{c2})/3$$

The inverter output voltage can be expressed as a function of the status of the switch, therefore, the equivalent circuit diagram of the circulation in inter- leaved parallel inverters as shown in **Figure 4**, where R is the sum of the resistance parameters in the inverter circuit.

The interleaved parallel inverter circulation loop differential equation (7)can be obtain from **Figure 4**:

$$2L\frac{di_{H0}}{dt}+2Ri_{H0}=(S_1-S_2)E \quad (4)$$

The two inverter modules of interleaved parallel inverters have the same current reference, and carrier wave shift 180°[6,8], therefore, it cannot guarantee that any time the switching state function S1-S2 is always 0, the circulation current must be exist. The waveform of circulation current is associated with (S1-S2), and take a switching cycle as example, the switching state of the two inverters are S_{x1}, S_{x2}, and its switching time as the shown in **Figure 5**.

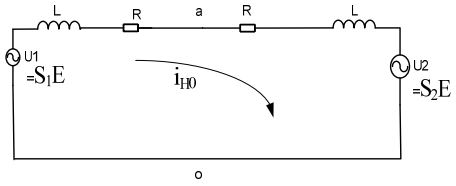

Figure 4. Circulation equivalent circuit diagram based on the interleaved parallel inverters.

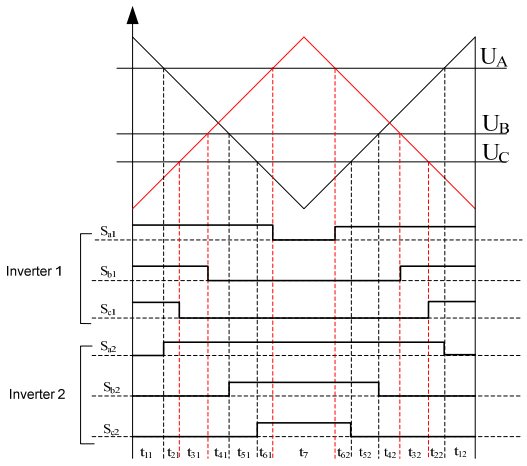

Figure 5. Within one switching cycle, the switching state of the two inverters Sx1, Sx2 and its switching time.

Table 1. The value of zero-sequence voltage U_{H0} in a switching cycle.

	U_1	U_2	U_1-U_2
t_{11} t_{12}	E	0	E
t_{21} t_{22}	E	E/3	2E/3
t_{31} t_{32}	2E/3	E/3	E/3
t_{41} t_{42}	E/3	E/3	0
t_{51} t_{52}	E/3	2E/3	-E/3
t_{61} t_{62}	E/3	E	-2E/3
t_7	0	E	-E

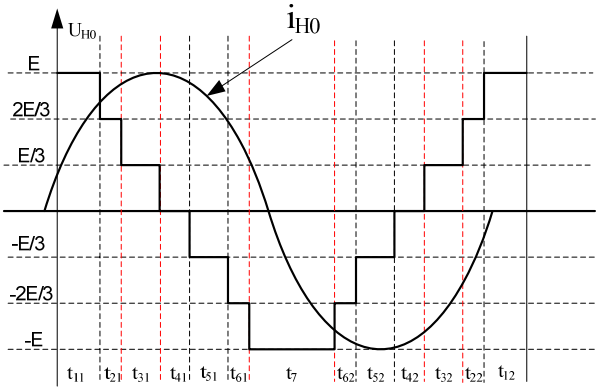

Figure 6. The waveform of zero-sequence circulation voltage U_{H0} in a switching cycle.

A switching cycle has been divided into 13 segments, in each segment, the zero-sequence voltage expressions U_{H0} are shown in **Table 2** (E as the DC bus voltage).

From **Table 1**, we can obtain the waveform of zero-sequence circulation voltage U_{H0} in the interleaved inverters in a switching cycle as shown in **Figure 6.**

The average value of the zero-sequence voltage is 0. In **Figure 4**, we can gain equivalent circuit diagram of the interleaved parallel inverters[6,8-9], and the amplitude of the zero-sequence current I_{H0} as

$$I_{H0}=\frac{E*t_7+\frac{2}{3}E*(t_{61}+t_{62})+\frac{1}{3}E*(t_{51}+t_{52})}{2(R+X_L)} \quad (5)$$

For interleaved parallel SPWM modulation, the two inverters must be work in two opposite of the zero vector state in each switching cycle, as it shows in **Figure 5**. It can be seen that the duration of t_7 which two opposite zero vectors overlap time in a switching cycle, is decided by the absolute value of the largest phase in three-phase

Modulation, With the MATLAB model is shown in **Figure 7**, the proportion of the zero vector action time in

a switching cycle is shown in **Figure 8**.

3. Mitigation of the Circulation Current

We can obtained this conclusion from the formula (5) and **Figure 8**: the zero sequence circulation current is ralated to the DC voltage E and the duration of two opposite zero vectors overlap time. Reducing the overlap time of two zero vectors of the inverter module can be reduced the amplitude of the circulation current, and increasing the filter inductors also can weaken the size of the circulation current, coupled inductor is a good choose to reduce the the circulation [2,8]. From **Figure 8** can be seen : the duration of two opposite zero vectors overlap time is inversely proportional to the modulation ratio, while the higher modulating ratio, the higher the utilization of the DC-bus voltage, which can also reduce the circulation current.

The inverter with high-frequency SPWM modulation, has high quality of the output waveform, but high switching frequency with more switching losses, and with low utilization of DC voltage. While the inverter with SVPWM modulation, it can get better output voltage waveform with not very high switching frequency, and maintaining a higher utilization rates of DC voltage. It gives the proportion of zero vector time within one switching cycle with different modulation method and modulation ratio in [4]. So SVPWM together with interleaving paralleled technology would be a better method to mitigate the circulation current.

In the formula (5), t_7 is the overlap time for the two opposite zero vector in the two inverter modules with interleaved parallel technology, When this is happening, the top switches of one module are connected to the positive dc rail and the bottom switches of the other module are connected to the negative dc rail. The three-phase currents will flow simultaneously from the dc bus capacitor through the top switches of one module, the filter inductors, the bottom switches of the other module, and back to the dc bus capacitor, as shown in **Figure 9**.

Theoretically, the zero-vectors (000 and 111) can be split apart and arranged appropriately in one switching cycle with other SVM schemes so that the effect of zero-vector overlap would be minimized or eliminated in a switching cycle. Uncertainties, however, exist in system transients and sector transition, where transition chattering is likely to occur because of the current ripple. Once the overlap is created, the zero-sequence will exist in at least one switching cycle before it can be corrected. Because the current loop operates as a feed back loop based on the existing current to perform the following actions, it can not be so fast as to eliminate the switching frequency current. And the overlap time between zero vectors (000 and 111) is decided to vector 000. Therefore, discontinuous space-vector modulation without using zero vector(000) to eliminate the zero vectors overlap time is an effective method for interleaved parallel system. **Figure 10** shows the principle of this modulation method, in a switching cycle, zero vector(000) using the two of the other switching cycle modulation vector and the inverse vector to synthesized. In the first sector, for example, the modulation vector of the inverter 1 is 111,110,100,000, and the effective time of each vector is

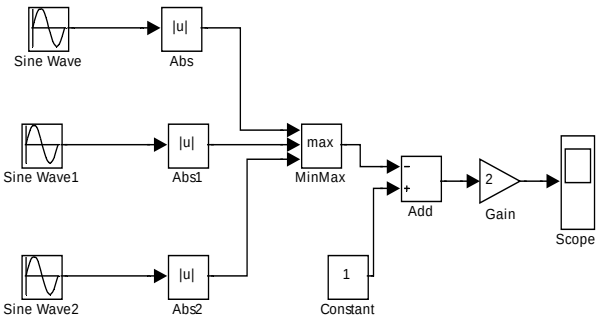

Figure 7. Simulation model of the proportion of zero vector action time.

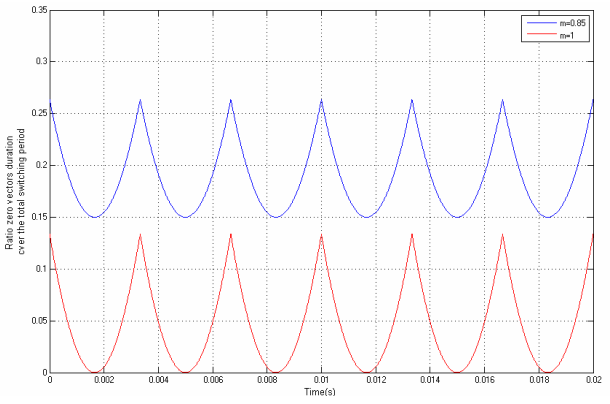

Figure 8. Simulated the proportion of zero vector for a sinusoidal reference voltage modulated in a switching cycle.

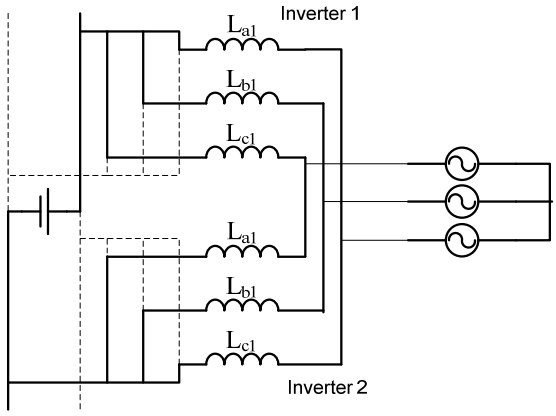

Figure 9. Example of the cross-current circulation when inverter 1 uses the zero vector v0(000) and inverter 2 uses v7(111).

t_1, t_2, t_3, t_4, a switching cycle of the zero vector effective time for the t_1, t_4, and a switching cycle within the modulation vector symmetrical distribution, while making $t_1=t_4=t_0$, select the effective time of the zero vector is divided into four equal periods of time and rearrange the duty cycles as the following,

$$t_2' = t_2 + \frac{t_0}{4}$$

$$t_3' = t_3 + \frac{t_0}{4}$$

$$t_1' = \frac{t_0}{2}$$

In the t_0 period, the vector(000) synthesize as shown in **Figure 10**.

Take the first sector as example, rearrange the order and the active time of space vector based on discontinuous space vector modulation without using zero vector (000) as shown in **Figure 11**.

With the application of discontinuous space vector modulation without using zero vector(000) in the first sector, a switching cycle is symmetrically divided into 14 segments, in each segment, the expression of zero sequence circulation voltage U_{H0} as shown in **Table 2.**

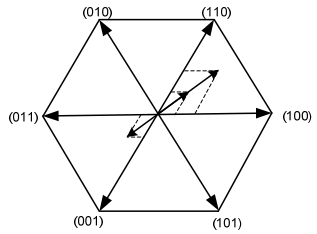

Figure 10. The principle of discontinuous space-vector modulation without using zero vector(000).

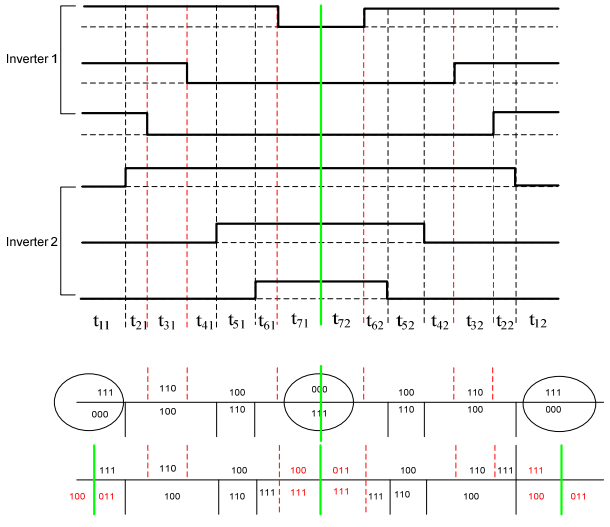

Figure 11. Switching signal of discontinuous space-vector modulation without using zero vector(000).

Table 2. The value of zero-sequence voltage U_{H0} in a switching cycle within discontinuous space vector modulation without using zero vector(000).

	U_1	U_2	U_1-U_2
t_{11}	E	2E/3	E/3
t_{21}	E	E/3	2E/3
t_{31}	2E/3	E/3	E/3
t_{41}	E/3	E/3	0
t_{51}	E/3	2E/3	-E/3
t_{61}	E/3	E	-2E/3
t_{71}	E/3	E	-2E/3
t_{72}	2E/3	E	-E/3
t_{62}	E/3	E	-2E/3
t_{52}	E/3	2E/3	-E/3
t_{42}	E/3	E/3	0
t_{32}	2E/3	E/3	E/3
t_{22}	E	E/3	2E/3
t_{12}	E	E/3	2E/3

From **Table 2**, we can obtain the waveform of zero-sequence circulation voltage U_{H0} with discontinuous space vector modulation without using zero vector(000) in a switching cycle as shown in **Figure 12**

Comparing **Figure 6** and **Figure 12**, the peak of zero-sequence circulation voltage U_{H0} in a switching cycle has been eliminated.

In addition to the switching circulation, the average of the cross-current theoretically is zero during a fundamental period, any small difference between the inverters determines a lower frequency circulation between them. The lower frequency zero-sequence current is removed by a current controller placed on zero-axis, which keeps a null average of the zero sequence current [7,10].

4. Simulation Results

In order to validate the proposed discontinuous SVM without using zero vector(000) in two parallel interleaved inverters, simulation has been built in Simulink. **Figure 13(a)** shows FFT analysis of the AC-side current in phase A as a single inverter, and **Figure 13(b)** illustrates FFT analysis of the AC-side current in phase A based on parallel interleaved inverters with discontinuous SVM without using zero vector(000).

Figure 14(a) shows the circulation waveform of phase A in two parallel inverters, and **Figure 14(b)** illustrates

the circulation waveform of phase A in parallel inverters based on interleaved discontinuous SVM without using zero vector(000).

5. Conclusions

The parallel interleaved technology in high-power applications, a single switch tube flow resistance value reduced by half, with the same current ripple request, the inductor size can be reduced by about 40%, it can also to improve the dynamic response time of the entire system. When two or more modules are connected directly to a dc bus and a three-phase source/load without using transformer isolation, the intended PWM interleave will cause the cross current in all the phases. This paper first introduces the cross current is ralated to the DC voltage E and the duration of two opposite zero vectors overlapped time. And then proposed the SVM without using zero vector(000), The simulation results have shown that the proposed SVM is feasible. It effectively eliminates the circulation current and simultaneously reduces the harmonic current. Simulation results validate the presented analysis.

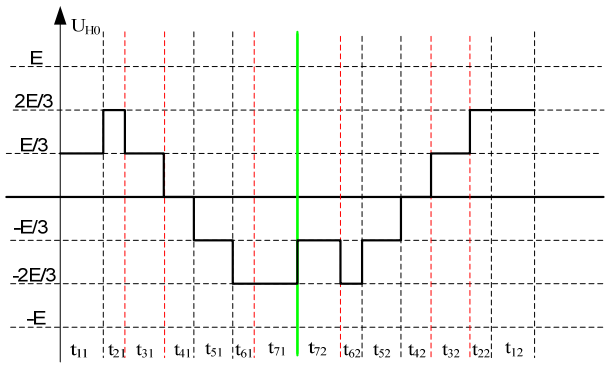

Figure 12. The waveform of zero-sequence circulation voltage U_{H0} in a switching cycle.

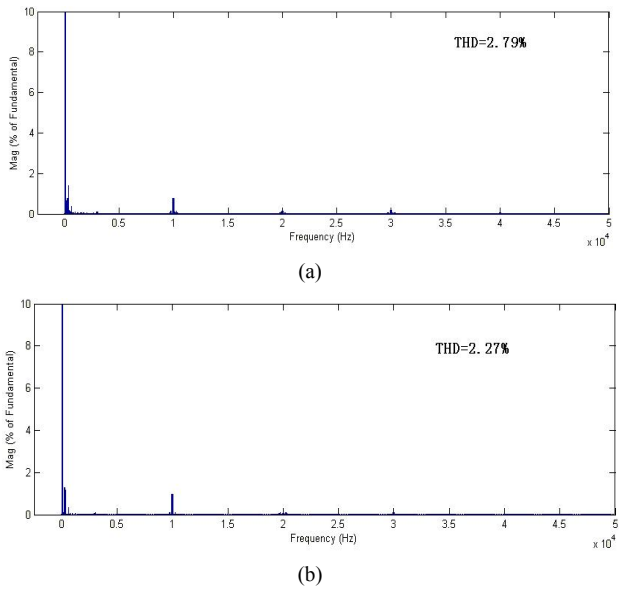

Figure 13. FFT analysis of AC-current in phase A. (a) Phase-A currents for single inverter. (b) Phase-A currents for two parallel interleaved inverters.

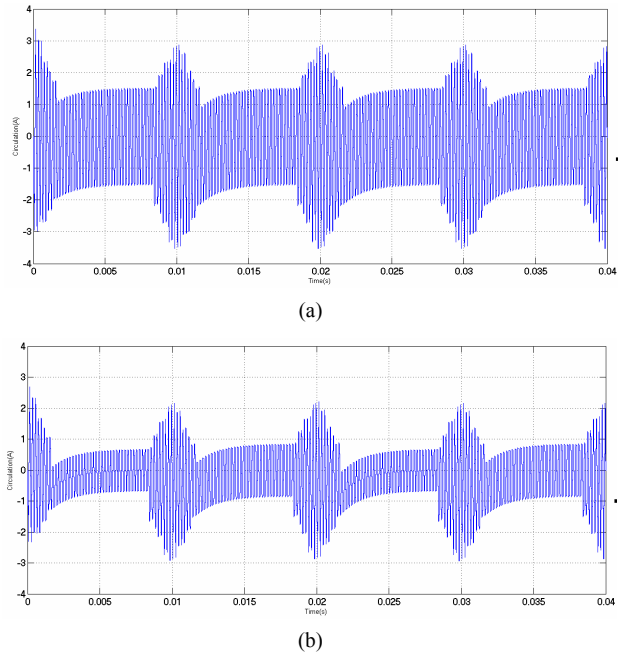

Figure 14. The circulation waveform of phase A (a) Phase-A currents for two parallel interleaved inverters without the proposed SVM . (b) Phase-A currents for two parallel interleaved inverters with the proposed SVM.

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