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Design and Evaluation of Solar Inverter for Different Power Factor Loads

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ABSTRACT

This paper analyzes and compares the performance of a new inverter topology with two types of input sources: 1) Solar PV source and 2) Ideal dc source (battery). The simulation is done in SIMULINK/MATLAB Software. It is shown that when the solar panel is connected, spikes are obtained in output voltage waveforms. These spikes are eliminated by inserting a capacitor. The capacitor is chosen for a particular power factor which is optimum with respect to cost, size and power quality. Total Harmonic Distortion, Active Power, Reactive Power, RMS Voltage and RMS Current are measured for different load power factor. Finally these results are compared with those obtained using battery with same input voltage magnitude. This Paper shows that for Solar Panel Circuit, THD, P and Q are less for 0.8 and above power factor, however below 0.8 PF, the THD, active and reactive power transfer are more. This means that the performance of Solar Panel in the proposed circuit topology is seen to be better as compared to the same circuit with battery within a range of power factor.

Keywords: H-Bridge Inverter; Level Module (LM); Power Quality; Power Factor; Total Harmonic Distortion (THD)

1. Introduction

Recently, renewable energy resources are becoming popular due to the depletion of conventional fuel sources and their negative impacts on the environment. Solar energy is one of these alternative renewable energy resources. It is converted to the electrical energy by photovoltaic (PV) arrays. PV arrays do not generate any toxic or harmful substances that pollute the environment and have long life. Another considerable feature of them is the requirement of low maintenance. Due to the development in photovoltaic technologies, the efficiency of the PV arrays has been improved. Therefore, studies on PV systems have increased gradually.

Multilevel inverters have received increasing interest for power conversion in high-power applications due to their lower harmonics, higher efficiency and lower voltage stress compared to two-level inverters. Multilevel inverters generate a staircase waveform. By increasing the number of levels in the output voltage, the harmonic content and therefore THD are reduced. Therefore, they produce high quality output voltage by increasing the level number. The level number can be easily increased. As a result, voltage stress is reduced and the output voltage wave shape move closure to the sinusoidal shape. In this study, a single phase multilevel inverter system is proposed. The principle of the proposed method will be explained for a 15-level inverter. However, the structure can be easily adapted to any number of levels.

2. Proposed Inverter

The proposed multi-level inverter system consists of Level Module, H-Bridge inverter, Solar PV Module as dc voltage source and RL load [1]. The proposed circuit with solar panel as source for two level modules is shown in **Figure 1**. The level of output voltage shape depends on the level module used in the circuit.

No. of output Levels

$$n = 2^{(m+1)} - 1,$$

where m is the no. of Level Module used [2].

The no. of switches used in the circuit

$$n_s = 2m + 4.$$

The input dc voltage fed to k^{th} module varies with particular module no. as:

$$V_k = 2^{(k-1)} \cdot V_b,$$

where $k = 1, 2, 3 \cdots m$ [3].

The Simulink model of the proposed circuit is shown in **Figure 2**. In the proposed circuit, 3 Level modules (LM),

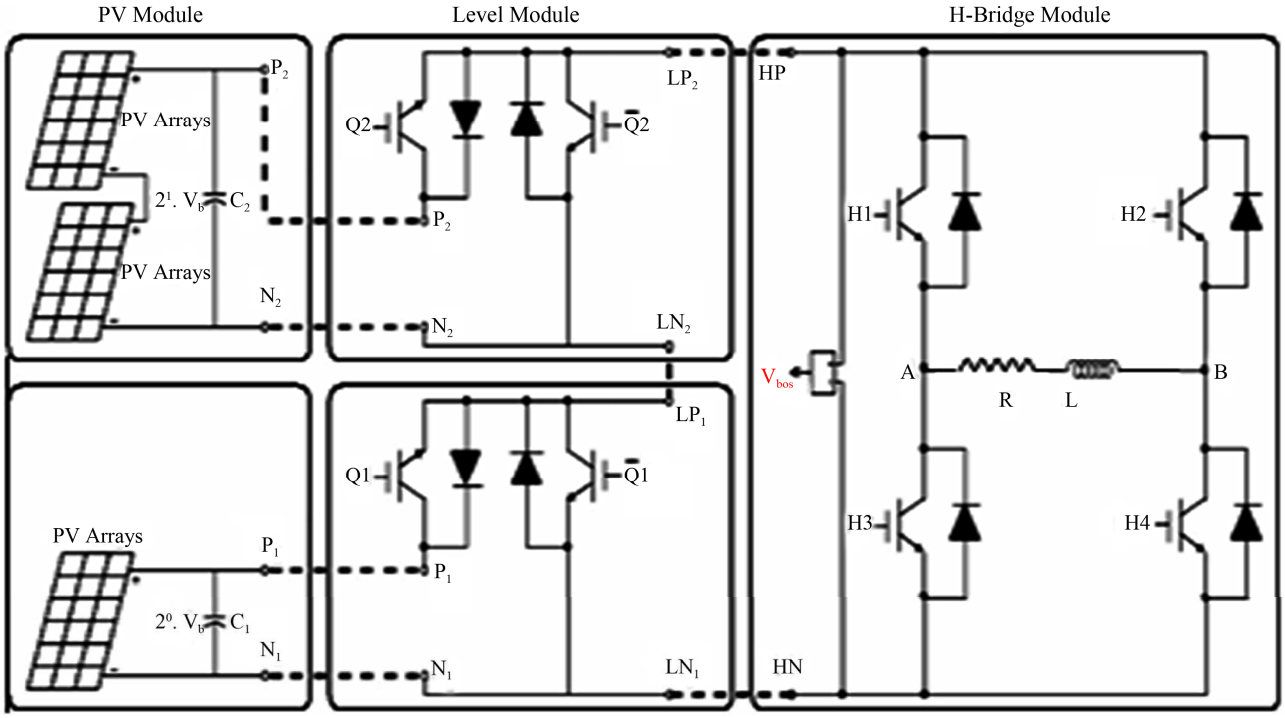

Figure 1. Proposed multilevel circuit of two level module.

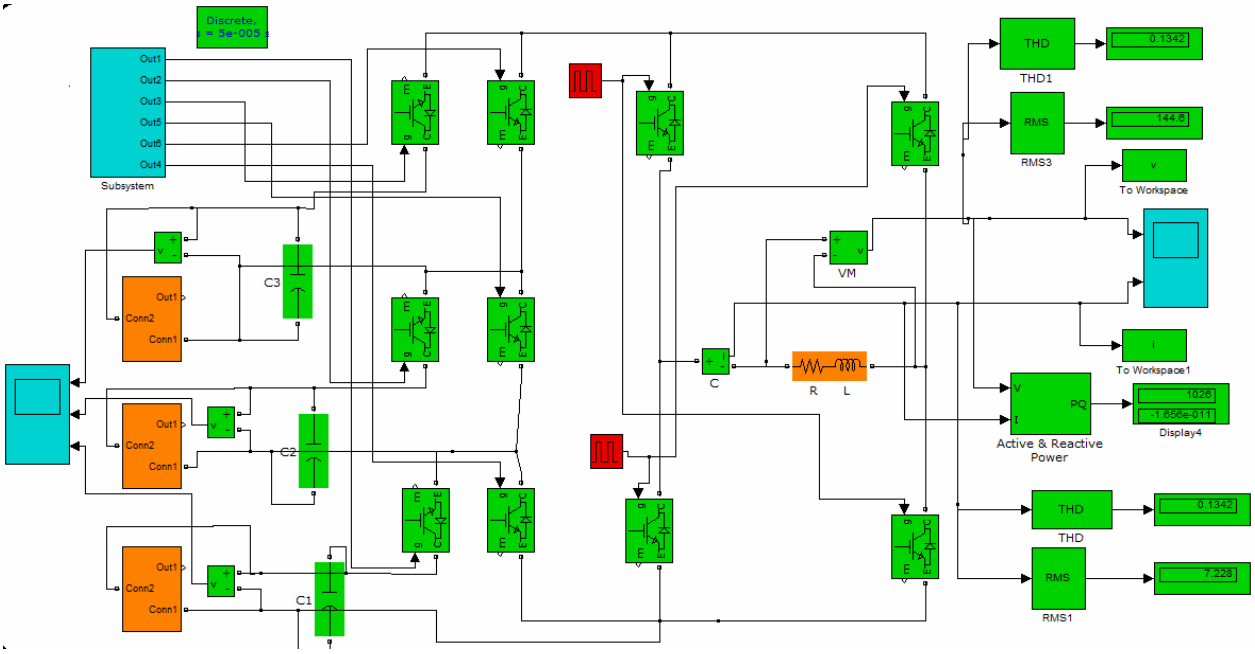

Figure 2. Matlab model for the proposed circuit.

1 H-Bridge inverter, and 3 Solar PV Array of output voltage $V_1(=V_b)$, $V_2(=2V_b)$ and $V_3(=4V_b)$ are used. Output wave has 15 levels and the total no. of switches used is 10. Total dc voltage used in the circuit is $7V_b$. The gate pulse for first LM switch Q_1 is a SPWM pulse having 7 pulses in each half cycle [4]. To find the gate pulse for second LM switch Q_2, this Q_1 is given to the clock of a negative edge triggered toggle flip flop. Further this Q_2 is given to the clock of another toggle flip flop to get gate pulses for third LM switch Q_3. The gate pulses for Q_1, Q_2 and Q_3 are shown in **Figure 3**.

The Simulink Model of PV Array used in the above circuit is shown in **Figure 4** [5]. The simulation is done for V_b = 32 Volt. V_b is measured when the PV model is

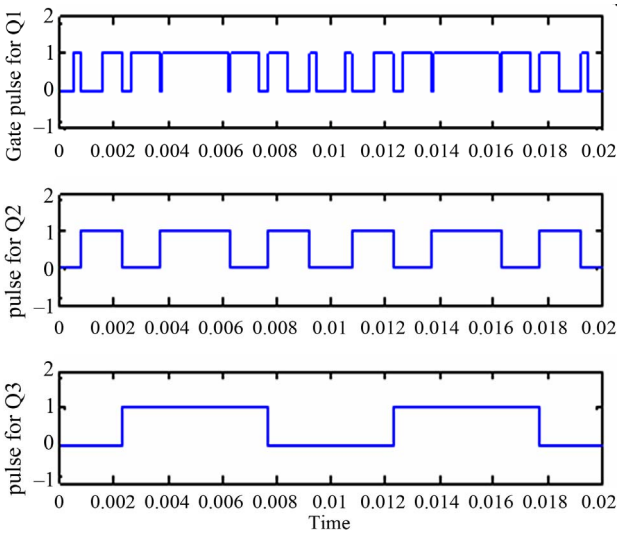

Figure 3. Gate pulses for Q1, Q2 and Q3 respectively.

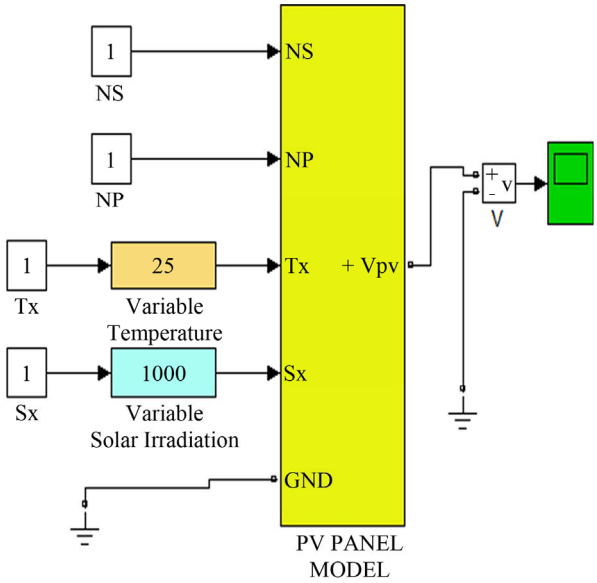

Figure 4. PV Array model used in the proposed circuit.

open circuited. When the PV Array is loaded, some fluctuations in PV Voltage are measured.

When the circuit is simulated, spikes occur in the output voltage wave which tends to deteriorate the power quality. To reduce these spikes, capacitors (C) across PV Array are connected as shown in **Figure 2**.

3. Simulation and Results

Solar Panel as a dc Source to the Inverter

The proposed circuit is simulated in SIMULINK/MATLAB software.

Panel Output Voltages are $V_1 (= V_b) = 32$ V , V_2 = 64 V and V_3 = 128 V, Z = 25 Ω.

Simulation is carried out for an RL load of impedance 25 Ω for different power factor [6]. It is shown that for Pure R (power factor = 1), there is no spike in output voltage wave. But as inductive nature of the load increases, spikes starts and continuously increase which deteriorates the Power Quality. The variation of THD in Load Voltage, RMS Voltage V_r, RMS Current I_r, Active Power P and Reactive Power Q with different load power factor (cosφ) is shown in **Table 1**.

Table 1 shows that as the power factor decreases from unity, spikes starts appearing and the magnitude of spike increases continuously and hence RMS Voltage increases. Also THD increases which results poor power quality. **As the THD increases with the decrement of power factor, THD will become more below 0.8 power factor**. Simultaneously Active Power P and Load Current decreases while Reactive Power Q increases with the inductive nature of the load.

The spikes obtained in Output Voltage wave for 0.975 and 0.8 power factor is shown in **Figures 5** and **6** respectively.

Calculating the Value of Capacitance

Spikes in the Output Voltage are reduced by inserting a

Table 1. Simulation results for proposed multilevel inverter for different power factor without capacitance.

PF Cosφ	V_r (V)	I_r (A)	P (W)	Q VAr	THD (%)	Spike (%)
1	144	5.76	815	0	13.43	**0**
0.975	145	5.74	797	181	16.15	**84**
0.95	148.5	5.76	784	257	26.2	**197**
0.925	155	5.8	772	317	39.0	**304**
0.9	164	5.84	762	369	52.1	**401**
0.85	187.6	5.95	745	461	77.9	**576**
0.80	216.2	6.1	732	548	102.2	**734**

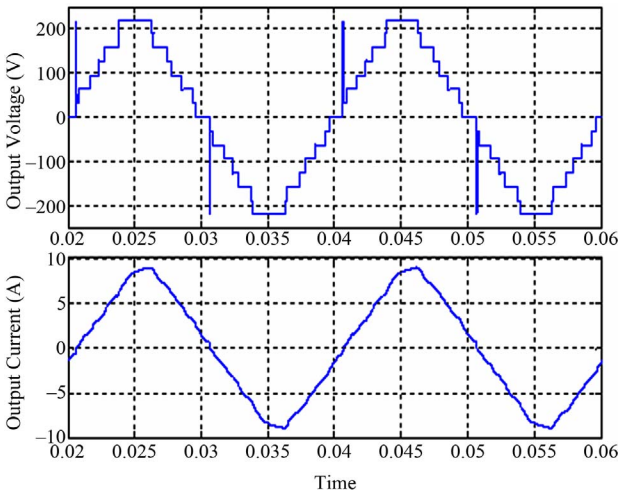

Figure 5. Output voltage and current wave for 0.975 power factor load.

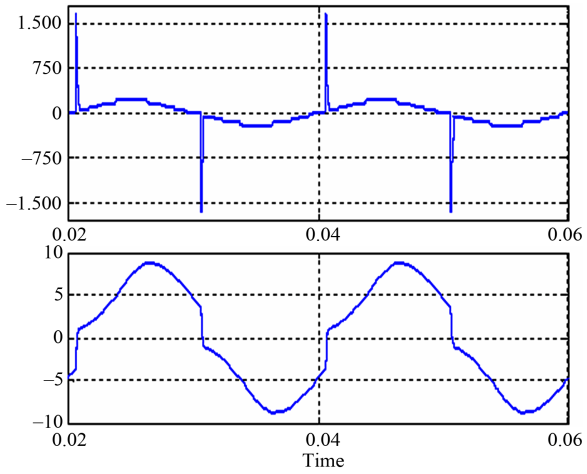

Figure 6. Output voltage and current wave for 0.8 power factor load.

Capacitance across PV Panel. The value of C should be optimum with respect to Cost, Size and power Quality. The variation of THD, V_r, I_r, P and Q with the capacitance value for 0.8 power factor (R = 20 Ω, L = 47.7 mH) is shown in **Table 2**.

$$\text{Percentage Spikes in output voltage} = \frac{\text{Magnitude of spike } (S_p)}{\text{Peak output voltage } (A)} \times 100\%.$$

For C = 10 μF,

Magnitude of spike = 198 V,

Output Peak voltage = 220 V.

Spike in output voltage

$$= \frac{198}{220} \times 100 = 90\% .$$

Table 2 shows that if the value of C increases, spikes decreases and hence RMS Voltage and THD decreases. But the decrement in magnitude of spike and hence in THD becomes very less beyond a certain value of C. So the optimum value with respect to Cost and Power Quality is taken as 50 μF. The voltage and current wave for C = 20 μF is shown in **Figure 7**.

Finally at C = 50 μF all the parameters are obtained for different value of power factor (keeping load impedance fixed at 25 Ω) as shown in **Table 3**.

Comparing **Tables 1** and **3** it is seen that for same power factor THD reduces up to a great extent after connecting a Capacitor across PV Panel. Load voltage and load current waveforms at C = 50 μF for 0.8 power factor is shown in **Figure 8**.

It is shown that as the power factor decreases, active power decreases and reactive power increases. Also, the variation of load current I_r with power factor is very small due to the fixed magnitude of impedance Z.

Table 2. Simulation results for proposed multilevel inverter for 0.8 power factor load.

C (μF)	V_r (V)	I_r (A)	P (W)	Q (VAr)	THD (%)	Spike (%)
5	164.2	6.27	781.3	586	32.2	**139**
10	159.2	6.12	765.3	574	24.5	**90**
20	154.8	6.1	743.7	557.7	17.7	**41**
30	152.5	6.0	727.5	545.6	14.9	**26.3**
50	149.6	5.93	704.3	528.1	12.8	**11.8**
60	149.1	5.92	699	524.8	12.6	**6.3**

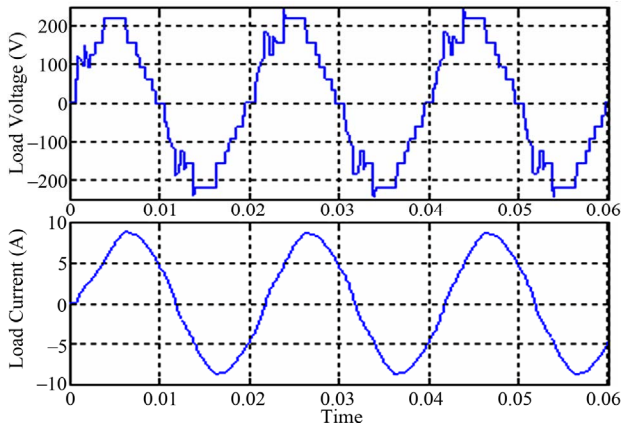

Figure 7. Load voltage and Load current wave at 0.8 power factor and 20 μF capacitance.

Table 3. Simulation results for proposed multilevel inverter for different power factor with C = 50 μF.

PF Cosφ	R (Ω)	L (mH)	V_r (V)	I_r (A)	P (W)	Q (VAr)	THD (%)
1	25	0	144.2	5.76	817	0	13.39
0.975	24.375	17.66	144.3	5.75	798	182	13.42
0.95	23.75	24.8	144.4	5.75	779	256	13.36
0.925	23.125	30.24	144.6	5.75	761	312	13.15
0.9	22.5	34.7	145.2	5.77	747	362	12.86
0.875	21.875	38.5	146	5.8	735	406	12.42
0.85	21.25	41.9	147	5.84	724	448	12.18
0.825	20.625	45	148	5.88	713	488	12.36
0.80	20	47.7	149.6	5.94	704	528	12.86
0.775	19.375	50.3	151.5	6.0	698	570	13.7
0.75	18.75	52.6	153.5	6.0	692	610	14.6
0.725	18.125	54.7	155.7	6.16	688	652	15.5
0.7	17.5	56.8	158	6.23	680	693	16.3

4. Battery as a dc Source to the Inverter

In the proposed circuit, batteries of same voltages are connected in place of Solar Panels. Simulation in SIMULINK/MATLAB software is done for same input dc voltages. Simulation Results are tabulated in **Table 4**.

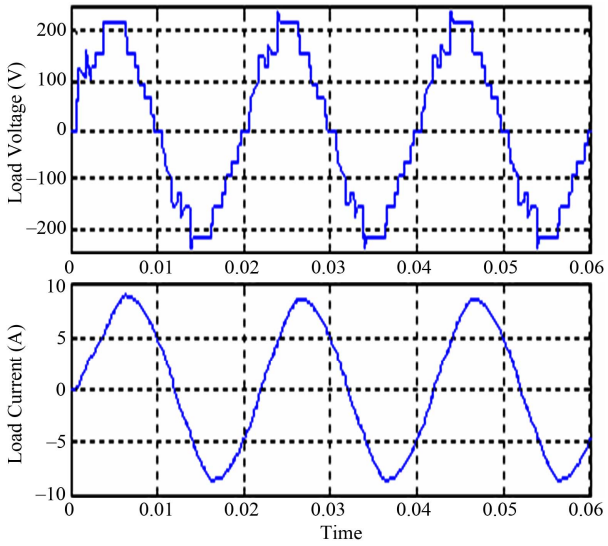

Figure 8. Load voltage and Load current wave at 0.8 power factor and 50 µF capacitance.

Table 4. Simulation results for proposed multilevel inverter with battery for different power factor.

PF Cosφ	R (Ω)	L mH	V_r (V)	I_r (A)	P (W)	Q (VAr)	THD (%)
1	25	0	146.5	5.86	843	0	13.44
0.975	24.375	17.66	146.5	5.83	822	187	13.44
0.95	23.75	24.8	146.5	5.82	801	263	13.44
0.925	23.125	30.24	146.5	5.82	779	320	13.44
0.9	22.5	34.7	146.5	5.82	758	367	13.44
0.875	21.875	38.5	146.5	5.82	738	408	13.44
0.85	21.25	41.9	146.5	5.82	717	444	13.44
0.825	20.625	45	146.5	5.81	695	476	13.44
0.80	20	47.7	146.5	5.81	675	505	13.44
0.775	19.375	50.3	146.5	5.81	653	532	13.44
0.75	18.75	52.6	146.5	5.81	632	557	13.44
0.725	18.125	54.7	146.5	5.82	612	580	13.44
0.7	17.5	56.8	146.5	5.81	590	602	13.44

For Z = 25 Ω, $V_1\left(=V_b\right)=32$ V, V_2 = 64 V and V_3 = 128 V.

Table 4 shows that for battery as a dc Source, the RMS voltage and THD are constant with the variation of load power factor. Active Power P is maximum at unity power factor while reactive power is zero. When power factor decreases, P decreases and Q increases while the load current is approximately the same (due to fixed Z). Load voltage and current waveforms for inverter with battery as dc source at 0.8 power factor is shown in **Figure 9**.

5. Comparison

In the proposed topology, for Solar PV as a dc source with capacitance, the THD is decreasing with the load power factor. For unity pf load, THD is 13.39% and for 0.8 PF load THD is 12.86%, *i.e.* Power Quality becomes better as the load becomes reactive. Below 0.8 PF load, the THD starts increasing. While the circuit having battery as source gives a constant THD of 13.44%. This means that for 0.8 or above power factor load the circuit with PV Panel gives better Power Quality. RMS current rating is approximately same for both the cases. The variation of THD with Load Power Factor for both the cases is shown in **Tables 3**, **4** and in **Figure 10**.

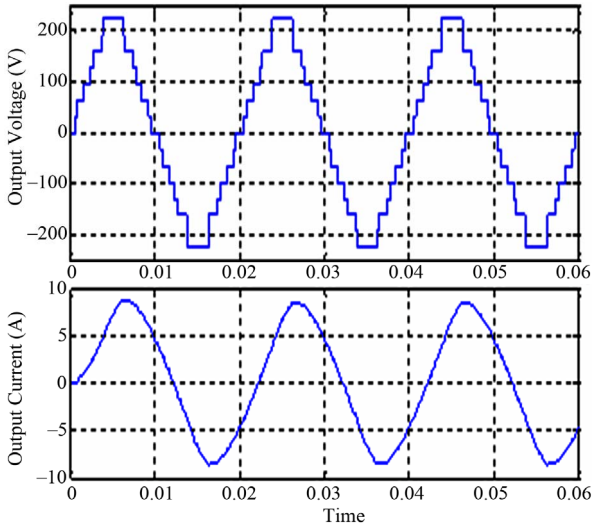

Figure 9. Load voltage and current at 0.8 PF for inverter circuit with battery as source.

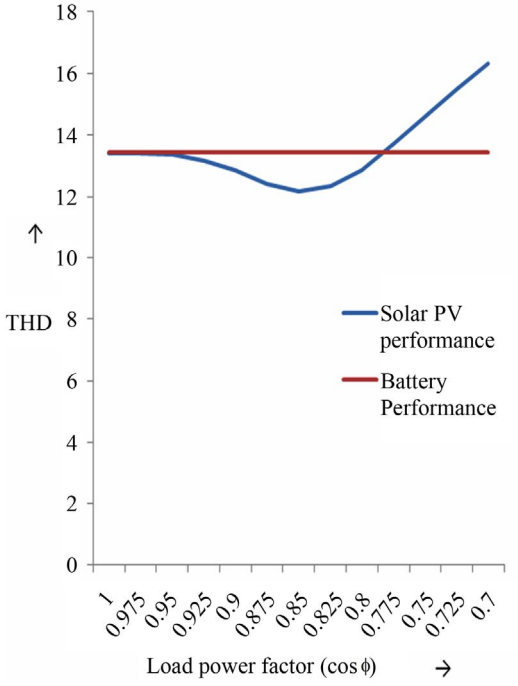

Figure 10. THD vs. load PF graph for proposed circuit with solar panel and battery as dc source.

Comparing the performances above, it is noted that for the power factor of 0.8 or above, the obtained THD is low for solar panel inverter circuit. However, the power obtained is more below 0.85 power factor. As far as active power and passive power as well as power quality are concerned, the solar panel will perform relatively better in the power factor range of 0.8 to 0.85.

6. Conclusions

In this paper, THD in load voltage, Active Power and Reactive Power are evaluated for a proposed inverter circuit with Solar Panel as a dc Source and also a battery using SIMULINK/MATLAB software. The performances are compared for different power factor loads keeping the dc input voltage same without using the filter. In both cases, THD present in load voltage may always be reduced below 5% by the use of filter. **The THD obtained from proposed inverter scheme is comparable to THD obtained from conventional inverter scheme but the no. of switches required is less in the proposed scheme.**

The overall observation is that in the range of pf from 0.8 to 0.85 the performance of PV panel connected inverter is superior to that with pure dc (battery) as input source.

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