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Harmonic Minimization in Seven Level Cascaded Multilevel Inverter Using Selective Harmonic Elimination PWM Techniques

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Abstract

This paper concentrates on enhancing the productivity of the multilevel inverter and nature of yield voltage waveform. Seven level lessened switches topology has been actualized with just seven switches. Essential Switching plan and Selective Harmonics Elimination were executed to diminish the Total Harmonics Distortion (THD) esteem. Selective Harmonics Elimination Stepped Waveform (SHESW) strategy is executed to dispense with the lower order harmonics. Fundamental switching plan is utilized to control the switches in the inverter. The proposed topology is reasonable for any number of levels. The harmonic lessening is accomplished by selecting fitting switching angles. It indicates would like to decrease starting expense and unpredictability consequently it is able for modern applications. In this paper, third and fifth level harmonics have been disposed of. Simulation work is done utilizing the MATLAB/Simulink programming results have been displayed to accept the hypothesis.

Keywords

Multilevel Inverter, PSIM, Fundamental Switching Scheme, Selective Harmonics Elimination

1. Introduction

These days, multilevel inverters have turned out to be more alluring for their utilization in high-voltage and high-control applications. In multilevel inverters, the fancied yield voltage is accomplished by appropriate blend of numerous low

dc voltage sources utilized at the input side. As the quantity of dc sources is expanded, the yield voltage turns out to be more like an immaculate sinusoidal waveform. The required dc sources can be browsed diversity of sources, for example, batteries, photovoltaic, fuel cells, capacitors, the rectified yield voltage of wind turbines, and other comparable dc sources [1] [2].

Diode-clamped multilevel converters are utilized as a part of customary high-control air conditioning motor drive applications like transports, pumps, fans, and plants. They have additionally been accounted for to be utilized as a part of a consecutive setup for regenerative applications [3]. Flying capacitor multilevel converters have been utilized as a part of high-transfer speed high-switching frequency applications. At long last, cascaded H-bridge multilevel converters have been connected where high power and power quality are fundamental. Moreover, one of the developing applications for multilevel motor drives is electric and half breed power trains.

For expanding voltage levels, the quantity of switches additionally will increment in number. Henceforth the voltage stresses and switching losses will increment and the circuit will get to be perplexing [4].

By utilizing the proposed topology number of switches will decrease altogether and thus the proficiency will improve [5]. In high power applications, the harmonic substance of the yield waveforms must be lessened however much as could be expected keeping in mind the end goal to maintain a strategic distance from bending in the matrix and to achieve the most extreme vitality efficiency [6]. The test connected with procedures is to acquire the systematic arrangements of the non-direct supernatural mathematical statements that contain trigonometric terms which actually show numerous arrangements of solutions [7]. For the most part, the lower order harmonics are bringing on more impacts when contrasted with the higher order harmonics. It is enormous test for any specialist to dispose of the third order harmonics utilizing straightforward methods, for a motor load its belongings are high. This paper proposes technique to dispense with lower order harmonics [8].

In this paper, Selective Harmonics Elimination procedure is utilized. In the proposed work, seven-level multilevel inverter with MOSFET is developed with selective harmonic elimination PWM to reduce the fifth and seventh order harmonics. The switching angles of the MOSFET are suitably controlled to produce the seven levels of output. The supernatural non-linear mathematical statements are fathomed utilizing the numerical procedure called Newton Raphson strategy. Cascaded H-bridge seven level inverter is displayed and harmonic examination is completed.

2. Cascaded Multilevel Inverter

A cascaded multilevel inverter has of number of H-Bridge inverter units associated in series and they are sustained from discrete DC sources. As the yield is

taken in series, the DC sources must be isolated from each other. Therefore, CHBMLIs is additionally been proposed to be utilized with energy components or photovoltaic clusters keeping in mind the end goal to accomplish higher voltage levels. The subsequent AC yield voltage is the expansion of the voltages produced by various H-Bridge cells. Each H-Bridge has the property to create three voltage levels as $+V_{dc}$, 0, $-V_{dc}$ by associating the DC source to the AC yield and by various mixes of four switches where V_{dc} is the input voltage of the H-Bridge. This proposed topology is utilized for getting seven-level cascaded H-Bridge multilevel inverter.

A seven-level multilevel inverter is acquired by cascading three H-bridge inverter circuits with every H-bridge nourished from a different DC source. The quantity of yield levels m in every stage is identified with number of H-bridge inverter unit's n by Equation (1).

$$m = 2n + 1 \tag{1}$$

where, m—is the No. of level of inverter, n—is the No. of full bridge connected in series.

Here number of levels (m) is seven thus number of full bridge inverter circuits associated in series is three which is known from the Equation (1). The single phase seven-level topology of cascaded H-bridge multilevel inverter is as appeared in Figure 1.

As each H-bridge is nourished with the same estimation of DC voltage it is called as symmetrical cascaded multilevel inverter. The DC voltages can be acquired from batteries; capacitors or power supplies. The phase yield voltage is the whole of three inverter yields. The seven-level yield waveform is acquired by various switching combinations. The switching design for single phase seven-level topology of cascaded H-bridge multilevel inverter is appeared in Table 1.

To get the said seven-level yield, the above switching pattern is utilized. The yield voltage waveform of seven-level inverter is as appeared in Figure 2 with α_1, α_2 and α_3 speaking to the switching angles which are utilized for harmonic reduction. By phase shifting the switching time of the positive and negative phase legs of the inverter, a quasi square waveform is generated by each full bridge as shown in Figure 2.

3. Selective Harmonic Elimination PWM

The selective harmonic elimination PWM technique is based on the fundamental switching frequency theory and dependent on the elimination of defined harmonic content orders. The primary thought of this technique depends on characterizing the switching angles of harmonic orders to dispense with and getting the Fourier series expansion of the yield voltage. This permit lower switching frequencies to be utilized which prompted lower switching misfortunes and higher effectiveness. When all is said in done Fourier series is given the Equation (2).

$$V(\omega t) = a_0 + \sum_{n=1}^{\infty}\left(a_n \cos n\omega t + b_n \sin n\omega t\right) \quad (2)$$

For this situation Fourier series extension of yield voltage waveform is given by "Equation (2)" as takes after,

$$V(\omega t) = \sum_{n=1}^{\infty}\left(b_n \sin n\omega t\right) \quad (3)$$

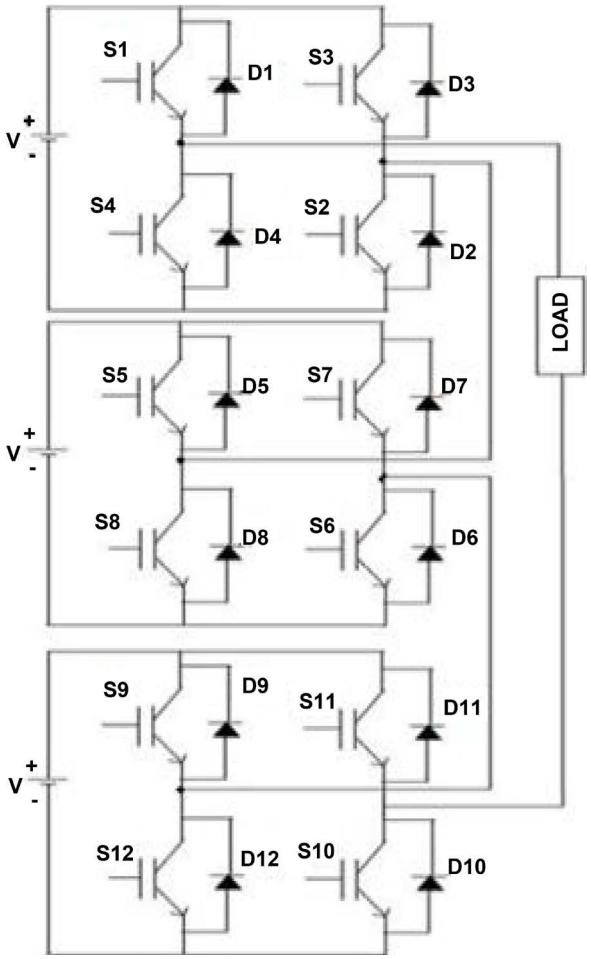

Figure 1. Single phase 7-level topology of cascaded H-bridge multi level inverter.

Table 1. Switching pattern for single phase 7-sevel Cascaded H bridge multilevel inverter.

VOLTAGE Van	SWITCHING STATES											
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
+V	1	1	0	0	0	1	0	1	0	1	0	1
+2V	1	1	0	0	1	1	0	0	0	1	0	1
+3V	1	1	0	0	1	1	0	0	1	1	0	0
0	0	1	0	1	0	1	0	1	0	1	0	1
−V	0	0	1	1	0	1	0	1	0	1	0	1
−2V	0	0	1	1	0	0	1	1	0	1	0	1
−3V	0	0	1	1	0	0	1	1	0	0	1	1

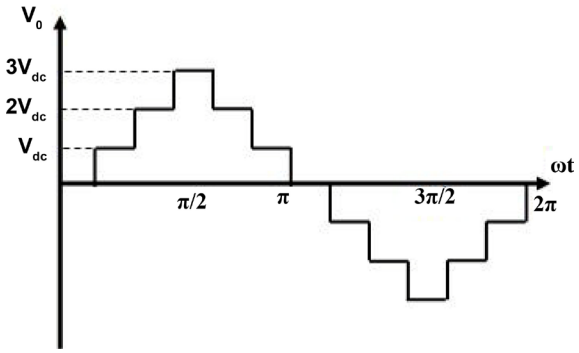

Figure 2. Yield voltage waveform of 7-level cascaded multilevel inverter.

where $a_n = a_0 = 0$ (due to quarter wave symmetry)

$$b_n = \frac{1}{\pi}\int_0^{2\pi} V_{dc} \sin n\omega t \mathrm{d}\omega t \tag{4}$$

From Figure 3 for quasi square wave Equation (4) is given as follows

$$b_n = \frac{2}{\pi}\int_{\alpha}^{\pi-\alpha} V_{dc} \sin n\omega t \mathrm{d}\omega t \tag{5}$$

On solving Equation (5) we get

$$b_n = \frac{4V_{dc}}{n\pi}\cos n\alpha \tag{6}$$

For seven level cascaded multilevel inverter for three DC sources comparison is given

$$b_n = \frac{4V_{dc}}{n\pi}\sum_{i=1}^{s}\cos\alpha_i \tag{7}$$

where n = 1, 5, 7 and s = 3 which speaks to number of DC sources. The goal of SHEPWM is to wipe out low order harmonics. In this number of harmonics that can be wiped out is equivalent to s − 1 *i.e.*, 2 so fifth and seventh harmonics are taken. Along these lines, to fulfill the fundamental harmonic component and to dispense with the fifth and seventh harmonics, Equation (7) is extended as three non-linear mathematical statements with three angles as gave in Equations ((8)-(10)).

$$b_1 = V_1 = \frac{4V_{dc}}{\pi}\left[\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3)\right] \tag{8}$$

$$b_5 = V_5 = \frac{4V_{dc}}{5\pi}\left[\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3)\right] \tag{9}$$

$$b_7 = V_7 = \frac{4V_{dc}}{7\pi}\left[\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3)\right] \tag{10}$$

In the mathematical statement (8)-(10), to dispense with fifth and seventh harmonic V_5 and V_7 are set to zero so that comparisons (11)-(13) are acquired. To decide the switching angles the accompanying mathematical statements must be illuminated,

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) = 3M \tag{11}$$

$$\cos(5\alpha_1)+\cos(5\alpha_2)+\cos(5\alpha_3)=0 \quad (12)$$

$$\cos(7\alpha_1)+\cos(7\alpha_2)+\cos(7\alpha_3)=0 \quad (13)$$

Here M speaks to modulation index changes from 0 to 1.The switching angles α_1, α_2 and α_3 must be not exactly $\pi/2$. The comparisons are fathomed by Newton Raphson strategy and resultant hypothesis in the writing. In any case, it is tedious and needs starting supposition for unraveling the mathematical statements. Consequently evolutionary algorithms are utilized for explaining this kind of non linear mathematical statements.

4. Simulation Results

The implementation of the Fuzzy logic Control technique is performed in the working platform of MATLAB The technique is implemented in a seven level H bridge inverter in such a way that it can eliminate the 3rd order and 5th order harmonics and so it can minimize the total harmonic distortion. Simulation of the seven level cascaded multilevel inverter when equal voltage values provided as the input to each of the H-bridges is done. Figure 3 shows the output voltage of the seven level cascaded MLI when equal voltage values are provided as input to each of the H-Bridges.

From the Figure 3, it is observed that the peak value of the output voltage of the MLI is about 329.4 V and its RMS value is 232.92 V. Figure 4 shows the harmonic spectrum of the output voltage of the seven level cascaded MLI. It can be noted that the total harmonic distortion on the output voltage is about 16.31%.

The output current of the seven level cascaded MLI when equal voltage values are provided as input to each of the H- Bridges is shown in the Figure 5. From the Figure 5, it is observed that the peak output current of the MLI is about 6.96 A and its RMS value is 4.92 A. Figure 6 shows the harmonic spectrum of the output current waveform. It can be noted that the total harmonic distortion on the output current is about 0.33%.

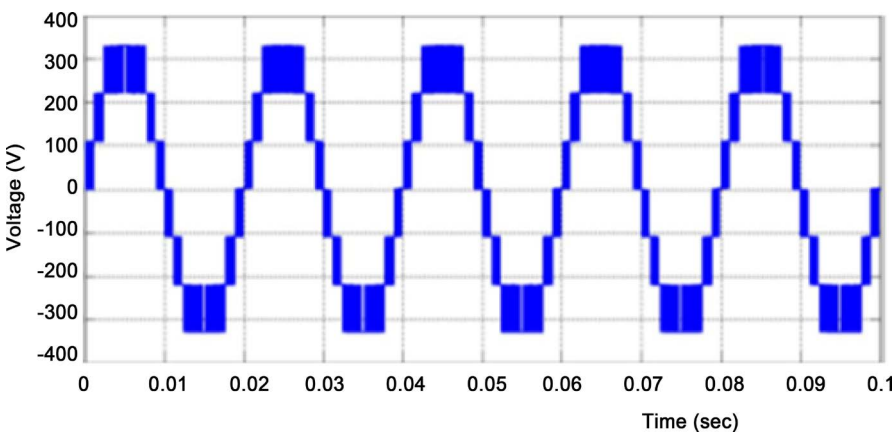

Figure 3. Seven level cascaded MLI output voltage without filter.

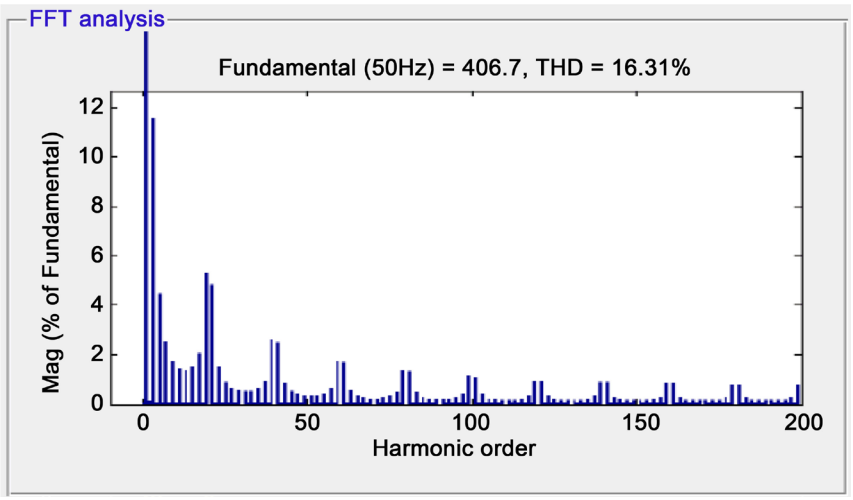

Figure 4. Harmonic Spectrum of the output voltage without filter.

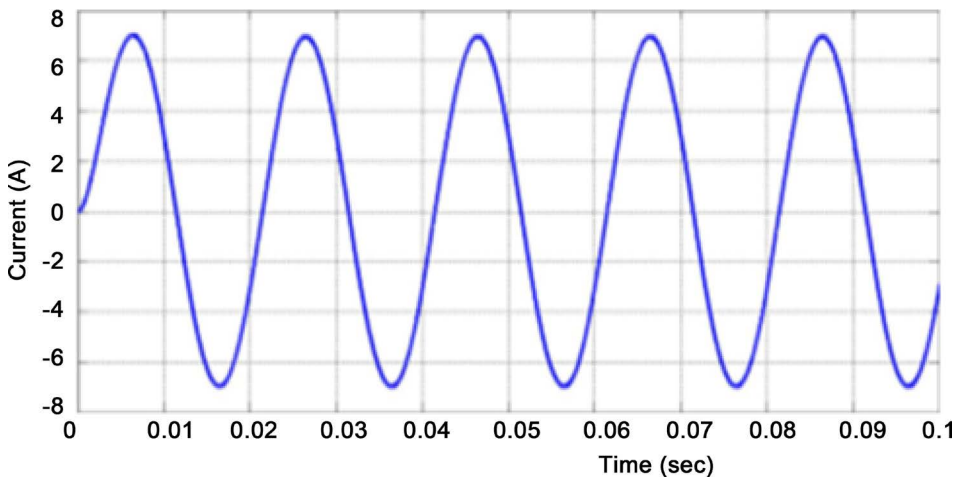

Figure 5. Seven level cascaded MLI current without filter.

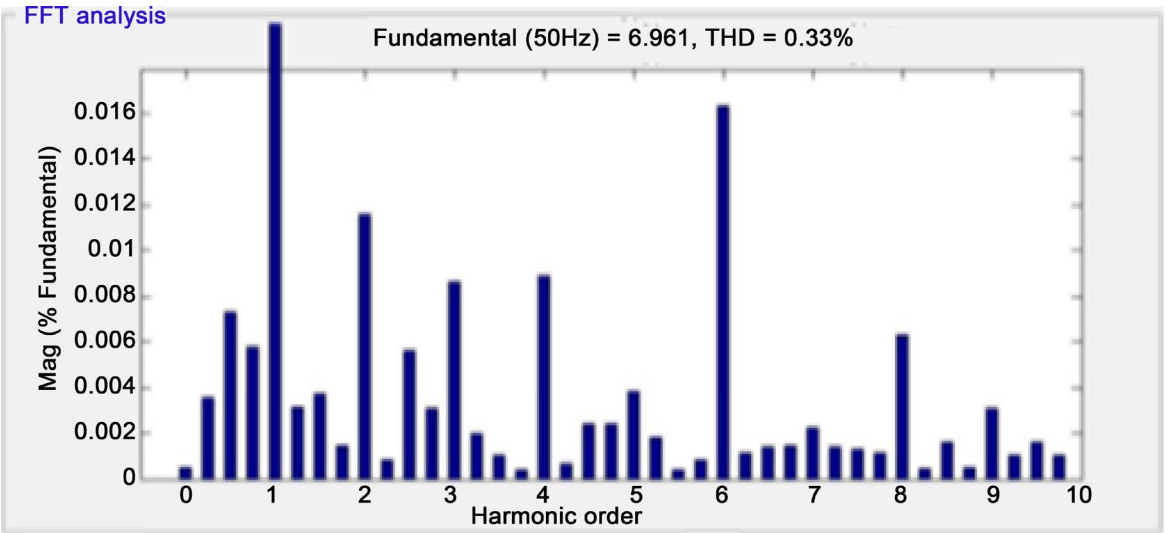

Figure 6. Harmonic Spectrum of the output current without filter.

In order to reduce the harmonic content on the MLI output, an LC filter is placed at the output stage of the inverter. The output voltage of seven level cascaded MLI is shown in the Figure 7. From the Figure 4.16 it is observed that the peak output voltage of the MLI is about 318.5 V and its RMS value is 225.21 V. Figure 8 shows the harmonic spectrum of the output voltage with filter. It can be noted that total harmonic distortion on the output voltage is reduced to 0.77% with an LC filter connected to MLI.

5. Conclusion

A summed up recipe of SHEPWM suitable for high power high voltage cascaded multilevel converters with equivalent DC voltage sources was proposed and exhibited in this paper. A complete simulation model of a cascaded multilevel inverter has been proposed utilizing MATLAB/Simulink programming. The proposed circuit produces required seven level yield voltages having low harmonics with decreased number of segments when contrasted with routine techniques. Harmonic spectrum for seven level yield voltages is examined to demonstrate its

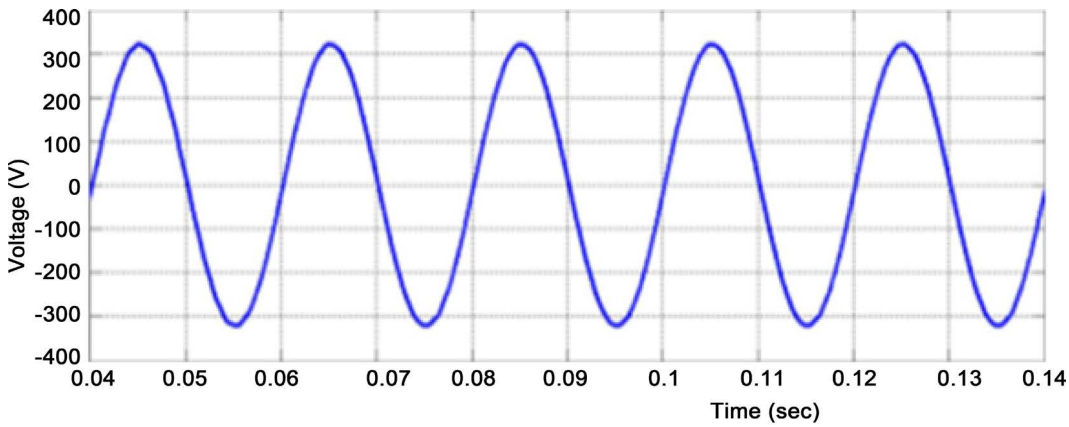

Figure 7. Seven level cascaded MLI output voltage with filter.

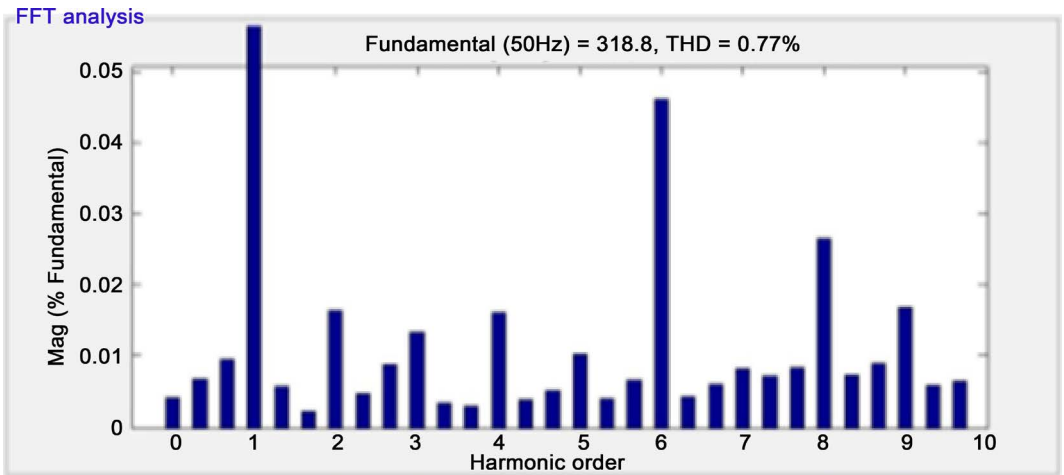

Figure 8. Harmonic Spectrum of the output current with filter.

productivity in diminishing yield harmonic segments. Simulated yield waveforms were appeared to demonstrate the unwavering quality and plausibility of the circuit. The Fast Fourier Transform (FFT) investigation is done to gauge the THD esteem. The FFT examination on the yield voltage waveform is appeared in Figure 4. From this it can be induced that the fifth and seventh harmonic is lessened and the THD acquired is 16.31%.

References

[1] Kavousi, A., Vahidi, B., Salehi, R., Bakhshizadeh, M., Farokhnia, N. and Fathi, S.H. (2012) Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters. *IEEE Transactions on Power Electronics*, **27**, 1689-1696. https://doi.org/10.1109/TPEL.2011.2166124

[2] Ahmadi, D., Zou, K., Li, C., Huang, Y. and Wang, J. (2011) A Universal Selective Harmonic Elimination Method for High-Power Inverters. *IEEE Transactions on Power Electronics*, **26**, 2743-2752. https://doi.org/10.1109/TPEL.2011.2116042

[3] Filho, F., Tolbert, L.M., Cao, Y. and Ozpineci, B. (2011) Real-Time Selective Harmonic Minimization for Multilevel Inverters Connected to Solar Panels Using Artificial Neural Network Angle Generation. *IEEE Transactions on Industry Applications*, **47**, 2117-2124. https://doi.org/10.1109/TIA.2011.2161533

[4] Sepahvand, H., Liao, J.S. and Ferdowsi, M. (2011) Investigation on Capacitor Voltage Regulation in Cascaded H-Bridge Multilevel Converters with Fundamental Frequency Switching. *IEEE Transactions on Industrial Electronics*, **58**, 5102-5111. https://doi.org/10.1109/TIE.2011.2130501

[5] Dahidah, M.S.A. and Agilities, V.G. (2008) Selective Harmonic Elimination PWM Control for Cascaded Multilevel Voltage Source Converters: A Generalized Formula. *IEEE Transactions on Power Electronics*, **23**, 1620-1630. https://doi.org/10.1109/TPEL.2008.925179

[6] Fei, W., Du, X. and Wu, B. (2008) A Generalized Half Wave Symmetry SHE-PWM Formulation for Multilevel Voltage Inverters. *IEEE Transactions on Industrial Electronics*, **5**, 3030-3038.

[7] Chiasson, J.N., Tolbert, L.M., McKenzie, K.J. and Du, Z. (2004) A Unified Approach to Solving the Harmonic Elimination Equations in Multilevel Converters. *IEEE Transactions on Power Electronics*, **19**, 478-500. https://doi.org/10.1109/TPEL.2003.823198

[8] Rodriguez, J., Lai, J.-S. and Peng, F.Z. (2002) Multilevel Inverters: A Survey of Topologies, Controls, and Applications. *IEEE Transactions on Industrial Electronics*, **49**, 724-738. https://doi.org/10.1109/TIE.2002.801052