Scientific Research Publishing

Circuits and Systems, 2016, 7, 4145-4153
http://www.scirp.org/journal/cs
ISSN Online: 2153-1293
ISSN Print: 2153-1285

New VD-DIBA-Based Single-Resistance-Controlled Sinusoidal Oscillator

Kanhaiya Lal Pushkar[1], Rajendra Kumar Goel[1], Kavya Gupta[1], Pinky Vivek[2], Javed Ashraf[2]

[1]Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, Rohini, India
[2]Department of Electronics and Communication Engineering, Al-Falah University, Faridabad, India
Email: klpushkar17@gmail.com, kumarrajendra2003@gmail.com, kavyagpt17@gmail.com, pinky.vivek18@gmail.com, jashraf.jmi@gmail.com

How to cite this paper: Pushkar, K.L., Goel, R.K., Gupta, K., Vivek, P. and Ashraf, J. (2016) New VD-DIBA-Based Single-Resistance-Controlled Sinusoidal Oscillator. *Circuits and Systems*, **7**, 4145-4153.
http://dx.doi.org/10.4236/cs.2016.713341

Received: May 5, 2016
Accepted: May 21, 2016
Published: November 18, 2016

Abstract

A new Single-Resistance-Controlled (SRC) sinusoidal oscillator using single Voltage Differencing-Differential Input Buffered Amplifier (VD-DIBA), only four passive components (two capacitors and two resistors), is presented. The proposed structure provides the following advantageous features: 1) independent control of oscillation frequency and condition of oscillation and 2) low active and passive sensitivities. The effects of non-idealities of the VD-DIBA on the proposed oscillator have also been investigated. The proposed SRC sinusoidal oscillator has been checked for robustness using Monte-Carlo simulation. SPICE simulation results have been included using 0.35 μm MIETEC technology to confirm the validity of the proposed SRC sinusoidal oscillator.

Keywords

Voltage Differencing-Differential Input Buffered Amplifier, Voltage-Mode Circuit, Sinusoidal Oscillator

1. Introduction

Numerous applications in control systems, signal processing, communications and instrumentation-measurement have been reported [1] [2] [3]. Recently, Biolek, Senani, Biolkova, and Kolka have introduced various modern active building blocks [4]. VD-DIBA is one of them which is emerging as a very flexible and versatile building block for analog signal processing/signal generation and has been used earlier for realizing a number of functions. Realization of oscillators, simulation of inductors and active filters has become important research areas in analog circuit design. Single Resistance

Controlled Sinusoidal Oscillators (SRCOs) employing different active building blocks have attracted considerable attention of the researchers due to their several advantages over traditional op-amp-based SRCOs, see [5]-[16] and the references cited therein.

The applications, advantages and usefulness of VD-DIBA have now been recognized in the technical literature. Biolek and Biolkova [17] have presented a first order Voltage-Mode (VM) all-pass filter using one VD-DIBA and a grounded capacitor. A high input impedance VM biquad filter employing two VD-DIBAs and two grounded capacitors has been presented by Jaikla, Biolek, Siripongdee and Bajer [18]. In [19] Pushkar, Bhaskar and Prasad proposed a new MISO-type VM universal biquad using single VD-DIBA, two capacitors and one resistor. The same authors [20] proposed another VM MISO-type universal biquad employing one VD-DIBA, two capacitors and a resistor. The uses of VD-DIBA in sinusoidal oscillator have been described in [21] [22] [23] [24]. In [21] Pushkar, Bhaskar and Prasad presented a SRCO using single VD-DIBA, two resistors and grounded capacitors offering independent control of condition of oscillation and frequency of oscillation. In [22] Bajer, Vavra and Biolek presented a VM quadrature oscillator using two VD-DIBAs and two grounded capacitors. Prasad, Bhaskar and Pushkar [23] proposed an electronically controllable oscillator employing two VD-DIBAs, two grounded capacitors and a grounded resistor, and oscillator offered independent control of condition of oscillation and frequency of oscillation. Bhaskar, Prasad and Pushkar [24] presented a fully uncoupled and electronically controllable sinusoidal oscillator using two VD-DIBAs, two grounded capacitors and two resistors, which offers totally uncoupled and independent control of condition of oscillation and frequency of oscillation. In [25] Prasad, Bhaskar and Pushkar presented new electronically controllable grounded and floating simulated inductance circuits. The grounded simulated inductance circuit uses two VD-DIBAs and a single grounded capacitor where as the floating simulated inductance circuit uses three VD-DIBAs and a grounded capacitor. Bhaskar, Prasad and Pushkar [26] proposed another electronically controllable grounded capacitor based grounded and floating simulated inductance circuit using VD-DIBAs. The grounded simulated inductance circuit employs single VD-DIBA, floating resistor and a grounded capacitor while the floating simulated inductance circuit employs two VD-DIBAs with one floating resistance and a grounded capacitor. The object of this paper is to present a new SRCO using a single VD-DIBA along with a bare minimum number of four passive components. The proposed structure offers: 1) independent control of Condition of Oscillation (CO) and Frequency of Oscillation (FO) and 2) low active and passive sensitivities. The validity of the proposed SRC sinusoidal oscillator has been confirmed by SPICE simulations using 0.35 μm MIETEC technology.

2. The Proposed New Oscillator Configuration

The circuit symbol and equivalent circuit model of the VD-DIBA are shown in **Figure 1(a)** and **Figure 1(b)** respectively. The model includes two controlled sources: the current source controlled by differential voltage $\left(V_+ - V_-\right)$ with the transconductance g_m

and the voltage source controlled by differential voltage $(V_z - V_v)$ with the unity voltage gain. The voltage-current relationship of input-output terminals of VD-DIBA can be described by the following matrix:

$$\begin{pmatrix} I_+ \\ I_- \\ I_z \\ I_v \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \end{pmatrix} \begin{pmatrix} V_+ \\ V_- \\ V_z \\ V_v \\ I_w \end{pmatrix} \tag{1}$$

The circuit analysis of proposed structure shown in Figure 2 yields the following characteristic equation (CE):

CE:

$$s^2 + s\left\{\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\frac{1}{R_1} - \frac{g_m}{C_1}\right\} + \frac{1}{R_1 R_2 C_1 C_2} = 0 \tag{2}$$

From Equation (2), the CO and FO can be given by:

CO:

$$\left\{\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\frac{1}{R_1} - \frac{g_m}{C_1}\right\} \le 0 \tag{3}$$

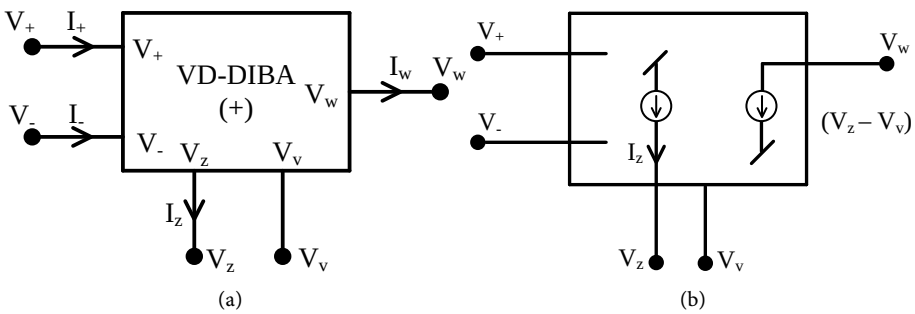

Figure 1. (a) Circuit symbol of VD-DIBA, (b) Equivalent circuit model of VD-DIBA.

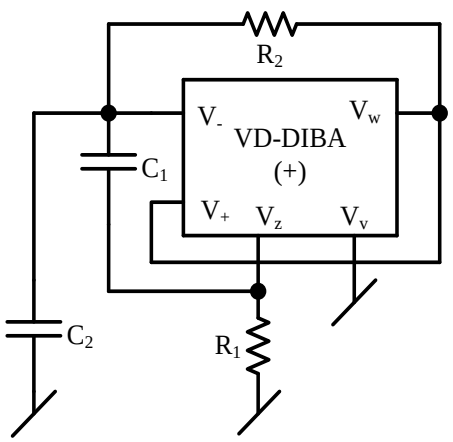

Figure 2. The proposed voltage-mode SRC sinusoidal oscillator configuration.

FO:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{R_1R_2C_1C_2}} \tag{4}$$

Therefore, the CO is electronically controllable independently by g_m while FO is independently controlled by resistor R_2.

3. Non-Ideal Analysis and Sensitivity Performance

Assuming, Z-terminal of the VD-DIBA have R_Z and C_Z as its parasitic resistance and parasitic capacitance respectively. Taking the non-idealities into account, namely the voltage of W-terminal $V_W = \left(\beta^+V_Z - \beta^-V_V\right)$ where $\beta^+ = 1-\varepsilon_p\ \left(\varepsilon_p \ll 1\right)$ and $\beta^- = 1-\varepsilon_n\ \left(\varepsilon_n \ll 1\right)$ denote the voltage tracking errors of Z-terminal and V-terminal of the VD-DIBA respectively, then the expressions for CE, CO and FO becomes:

CE:

$$\begin{aligned} &s^2\left(C_1C_2 + C_1C_z + C_2C_z\right) + s\left\{\left(C_1 + C_2\right)\left(\frac{1}{R_1} + \frac{1}{R_z}\right) + \left(C_1 + C_z\right)\frac{1}{R_2}\right. \\ &\left. + g_mC_1 - \beta^+\left(g_m\left(C_1 + C_2\right) + \frac{C_1}{R_2}\right)\right\} + \left(\frac{1}{R_zR_2} + \frac{1}{R_1R_2}\right) = 0 \end{aligned} \tag{5}$$

CO:

$$\left\{\left(C_1 + C_2\right)\left(\frac{1}{R_1} + \frac{1}{R_z}\right) + \left(C_1 + C_z\right)\frac{1}{R_2} + g_mC_1 - \beta^+\left(g_m\left(C_1 + C_2\right) + \frac{C_1}{R_2}\right)\right\} \le 0 \tag{6}$$

FO:

$$\omega_0 = \sqrt{\frac{R_1 + R_z}{R_1R_2R_z\left(C_1C_2 + C_1C_z + C_2C_z\right)}} \tag{7}$$

The left hand side of Equation (3) with the component values shown in this section turns out to be −0.060477 which is in accordance with Equation (3) (<0). On the other hand, the left hand side of Equation (6) using the components and parasitic values turns out to be −2.2588. It is, therefore, seen that both values are negative and satisfy the Equation (3) and Equation (6).

The active and passive sensitivities can be calculated as:

$$S_{R_z}^{\omega_o} = -\frac{1}{2}\left(\frac{R_1}{R_1 + R_z}\right),\ S_{R_1}^{\omega_o} = -\frac{1}{2}\left(\frac{R_z}{R_1 + R_z}\right),\ S_{R_2}^{\omega_o} = -\frac{1}{2},\ S_{C_1}^{\omega_o} = -\frac{1}{2}\frac{1}{1 + \dfrac{C_2C_Z}{C_1\left(C_Z + C_2\right)}} \tag{8}$$

$$S_{C_z}^{\omega_o} = -\frac{1}{2}\frac{1}{1 + \left(\dfrac{C_1C_2}{C_z\left(C_1 + C_2\right)}\right)},\ S_{C_2}^{\omega_o} = -\frac{1}{2}\frac{1}{1 + \left(\dfrac{C_1C_Z}{C_2\left(C_Z + C_1\right)}\right)} \tag{9}$$

In the ideal case, the various sensitivities of ω_0 with respect to R_1, R_2, C_1, C_2, C_z and R_z are found to be

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2},\ S_{C_z}^{\omega_0} = S_{R_z}^{\omega_0} = 0 \tag{10}$$

Considering the typical values of various parasitic e.g. $C_z = 0.81$ pF, $R_z = 53$ kΩ, $\beta^+ = \beta^- = 1$ along with $C_1 = C_2 = 100$ pF, $R_1 = R_2 = 8$ kΩ, the various sensitivities are found to be $S_{C_1}^{\omega_0} = -0.49$, $S_{C_2}^{\omega_0} = -0.49$, $S_{C_Z}^{\omega_0} = -0.01$, $S_{R_1}^{\omega_0} = -0.43$, $S_{R_2}^{\omega_0} = -0.5$ and $S_{R_Z}^{\omega_0} = -0.06$ which are all quite low.

4. Simulation Results

The proposed SRC sinusoidal oscillator is simulated using CMOS VD-DIBA (as shown in Figure 3) to verify its theoretical analysis. The passive elements were selected as $C_1 = C_2 = 100$ pF, $R_1 = R_2 = 8$ kΩ. The transconductance of VD-DIBA was controlled by bias voltage V_{B1}. The transient response of the proposed SRCO showing the buildup of oscillations for above component values is shown in Figure 4(a). A typical steady state

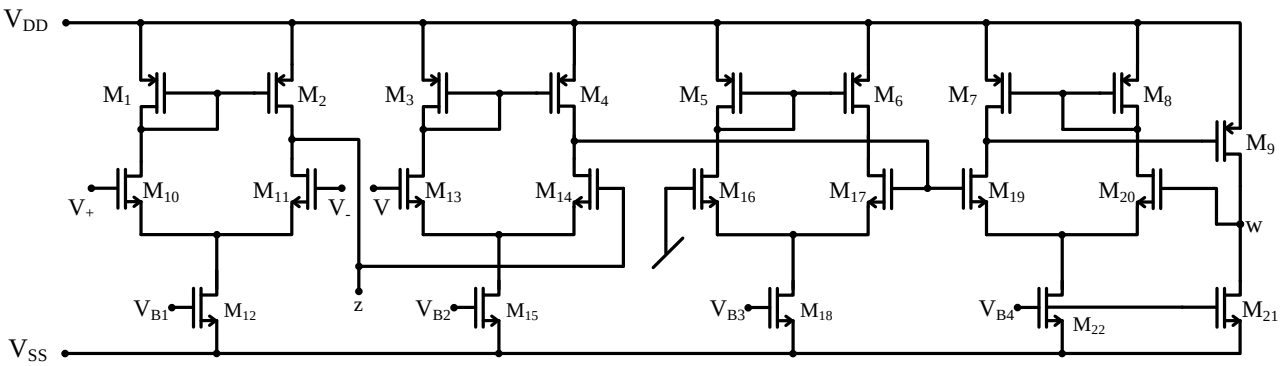

Figure 3. A CMOS Implementation of VD-DIBA, $V_{DD} = -V_{SS} = 2$ V, $V_{B1} = -0.46$ V, $V_{B2} = V_{B3} = -0.22$ V and $V_{B4} = -0.9$ V.

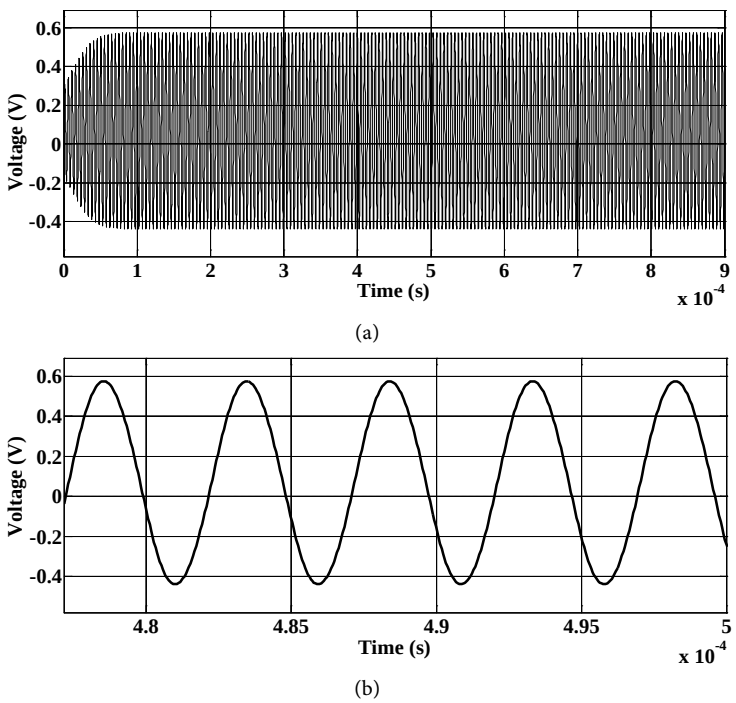

Figure 4. Waveforms of proposed SRCO: (a) Transient output, (b) Steady state output.

waveform generated by the oscillator for the frequency 203.01 kHz (for the same component values) is shown in Figure 4(b). Figure 5 shows the frequency response of the output, where the Total Harmonic Distortion (THD) is found to be 1.72%. The oscillator circuit of Figure 2 has been checked for robustness using Monte-Carlo simulation, the sample results have been shown in Figure 6 which confirm that, for ±5% variation in the value of R_1, the value of oscillation frequency remains close to its normal value of 204.459 kHz and hence almost unaffected by change in R_1. Figure 7 shows the variability

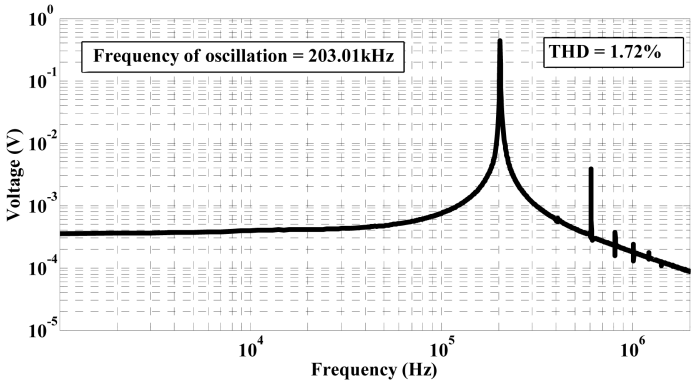

Figure 5. Frequency response of the output.

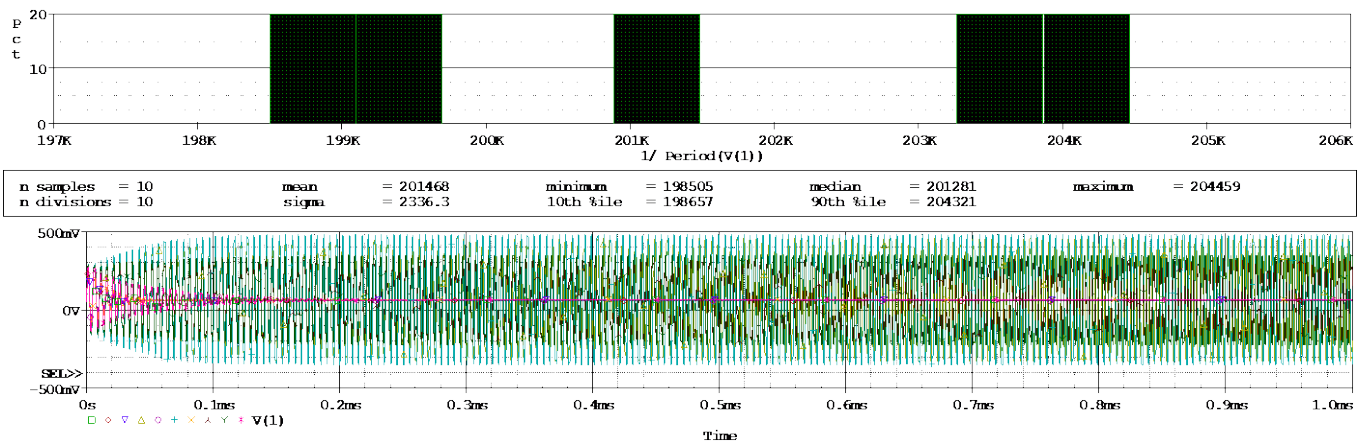

Figure 6. Monte Carlo analysis of proposed SRCO.

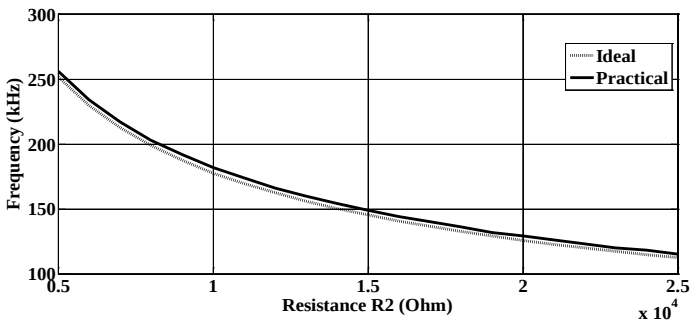

Figure 7. Variation of the oscillation frequency of the proposed SRCO with resistance R_2.

of the frequency with resistance R_2 varied from 5 kΩ to 25 kΩ. These results, thus, confirm the validity of the proposed structure. A comparison with other previously known SRCOs using different active building blocks has been given in Table 1.

The CMOS VD-DIBA is implemented using 0.35 μm MIETEC technology. The various transistor model parameters used are listed in Table 2 and W/L ratios (aspect ratios) of the MOSFETs used in Figure 3 are given in Table 3.

5. Conclusions

A new application of VD-DIBA has been proposed in the realization of SRCO. The proposed structure employs a minimum possible number of passive elements (namely,

Table 1. A comparison with other previously known SRCOs using different active building blocks.

Reference	Active Component(s)	Grounded Capacitors	Floating Capacitors	Resistors	CO and FO Independently Controllable
[5]	1	1	1	3	YES
[6]	2	2	0	3	YES
[7]	1	1	1	3	YES
[8]	1	1	1	3	YES
[9]	2	2	0	3	YES
[10]	1	2	0	4	NO
[11]	1	2	0	3/2	YES
[12]	1	2	0	3	YES
[13]	1	1 (virtually grounded)	1	3	YES (only in second topology of Table 2)
[14]	1	1 (virtually grounded)	1	3	NO
[15]	1	2	0	2	YES
[16]	1	1	1	2	YES
[21]	1	2	0	2	YES
[22]	3	2	0	0	YES
[23]	2	2	0	1	YES
[24]	2	2	0	2	YES (fully uncoupled)
Proposed	1	1	1	2	YES

Table 2. The transistor model parameters.

.MODEL N NMOS (LEVEL = 3 TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871 PHI = 0.7 VTO = 0.5445549 DELTA = 0 UO = 436.256147 ETA = 0 THETA = 0.1749684 KP = 2.055786E-4 VMAX = 8.309444E4 KAPPA = 0.2574081 RSH = 0.0559398 NFS = 1E12 TPG = 1 XJ = 3E-7 LD = 3.162278E-11 WD = 7.046724E-8 CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO = 1E-10 CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504 CJSW = 3.777852E-10 MJSW = 0.3508721)

.MODEL P PMOS (LEVEL = 3 TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.4083894 PHI = 0.7 VTO = −0.7140674 DELTA = 0 UO = 212.2319801 ETA = 9.999762E-4 THETA = 0.2020774 KP = 6.733755E-5 VMAX = 1.181551E5 KAPPA = 1.5 RSH = 30.0712458 NFS = 1E12 TPG = −1 XJ = 2E-7 LD = 5.000001E-13 WD = 1.249872E-7 CGDO = 3.09E-10 CGSO = 3.09E-10 CGBO = 1E-10 CJ = 1.419508E-3 PB = 0.8152753 MJ = 0.5 CJSW = 4.813504E-10 MJSW = 0.5)

Table 3. Aspect ratios of the MOSFETs.

Transistor	W/L (μm)
M1-M6	14/1
M7-M9	14/0.35
M10-M18	4/1
M19-M22	7/0.35

two resistors and two capacitors) and offers independent control of FO through the resistor R_2 and CO through the transconductance g_m. The proposed structure has low active and passive sensitivities. The robustness of the proposed SRCO circuit has been confirmed by the Monte-Carlo analysis. The workability of proposed structure has been confirmed by SPICE simulation with 0.35 μm MIETEC technology. However, any SRCO employing single VD-DIBA with both grounded capacitors and offering independent electronic control of FO is open to investigation.

References

[1] Senani, R. (1985) New Types of Sine Wave Oscillators. *IEEE Transactions on Instrumentation and Measurement* (*USA*), **34**, 461-463. http://dx.doi.org/10.1109/TIM.1985.4315370

[2] Senani, R. and Bhaskar, D.R. (1991) Single-Op-Amp Sinusoidal Oscillators Suitable for Generation of Very Low Frequencies. *IEEE Transactions on Instrumentation and Measurement* (*USA*), **40**, 777-779. http://dx.doi.org/10.1109/19.85353

[3] Bhaskar, D.R. and Senani, R. (2006) New CFOA-Based Single-Element-Controlled Sinusoidal Oscillators. *IEEE Transactions on Instrumentation and Measurement* (*USA*), **55**, 2014-2021. http://dx.doi.org/10.1109/TIM.2006.884139

[4] Biolek, D., Senani, R., Biolkova, V. and Kolka, Z. (2008) Active Elements for Analog Signal Processing; Classification, Review and New Proposals. *Radioengineering*, **17**, 15-32.

[5] Lee, C.T. and Wang, H.Y. (2001) Minimum Realization for FTFN-Based SRCO. *Electronics Letters, IEE* (*UK*), **37**, 1207-1208. http://dx.doi.org/10.1049/el:20010856

[6] Bhaskar, D.R. and Senani, R. (1993) New Current-Conveyor-Based Single-Resistance-Controlled/Voltage-Controlled Oscillator Employing Grounded Capacitors. *Electronics Letters, IEE* (*UK*), **29**, 612-614. http://dx.doi.org/10.1049/el:19930410

[7] Celma, S., Martinez, P.A. and Carlosena, A. (1992) Minimal Realisation for Single Resistor Controlled Sinusoidal Oscillator Using Single CCII. *Electronics Letters*, **28**, 443-444. http://dx.doi.org/10.1049/el:19920279

[8] Singh, V.K., Sharma, R.K., Singh, A.K., Bhaskar, D.R. and Senani, R. (2005) Two New Canonic Single-CFOA Oscillators with Single Resistor Controls. *IEEE Transactions on Circuits and Systems II: Express Brief* (*USA*), **52**, 860-864. http://dx.doi.org/10.1109/TCSII.2005.853964

[9] Bhaskar, D.R. (1999) Single Resistance Controlled Sinusoidal Oscillator Using Single FTFN. *Electronics Letters, IEE* (*UK*), **35**, 190-191. http://dx.doi.org/10.1049/el:19990161

[10] Bhaskar, D.R. (2002) Grounded-Capacitor SRCO Using Only One PFTFN. *Electronics Letters, IEE* (*UK*), **38**, 1156-1157. http://dx.doi.org/10.1049/el:20020839

[11] Aggarwal, V., Kilinc, S. and Cam, U. (2006) Minimum Component SRCO and VFO Using a Single DVCCC. *Analog Integrated Circuits and Signal Processing*, **49**, 181-185.

http://dx.doi.org/10.1007/s10470-006-9364-2

[12] Gupta, S.S. and Senani, R. (2000) Grounded-Capacitor Current-Mode SRCO: Novel Application of DVCCC. *Electronics Letters*, *IEE* (*UK*), **36**, 195-196. http://dx.doi.org/10.1049/el:20000240

[13] Ozcan, S., Toker, A., Acar, C., Kuntman, H. and Cicekoglu, O. (2000) Single Resistance-Controlled Sinusoidal Oscillators Employing Current Differencing Buffered Amplifier. *Microelectronics Journal*, **31**, 169-174. http://dx.doi.org/10.1016/S0026-2692(99)00113-5

[14] Cam, U. (2002) A Novel Single-Resistance-Controlled Sinusoidal Oscillator Employing Single Operational Transresistance Amplifier. *Analog Integrated Circuits and Signal Processing*, **32**, 183-186. http://dx.doi.org/10.1023/A:1019586328253

[15] Biolek, D., Keskin, A.U. and Biolkova, V. (2010) Grounded Capacitor Current Mode Single Resistance-Controlled Oscillator Using Single Modified Current Differencing Transconductance Amplifier. *IET Circuits Devices System*, **4**, 496-502. http://dx.doi.org/10.1049/iet-cds.2009.0330

[16] Prasad, D., Bhaskar, D.R. and Singh, A.K. (2008) Realisation of Single-Resistance-Controlled Sinusoidal Oscillator: A New Application of the CDTA. *WSEAS Transactions on Electronics*, **6**, 257-259.

[17] Biolek, D. and Biolkova, V. (2009) First-Order Voltage-Mode All-Pass Filter Employing One Active Element and One Grounded Capacitor. *Analog Integrated Circuits and Signal Processing* (*USA*), **65**, 123-129. http://dx.doi.org/10.1007/s10470-009-9435-2

[18] Jaikla, W., Biolek, D., Siripongdee, S. and Bajer, J. (2014) High Input Impedance Voltage-Mode Biquad Filter Using VD-DIBAs. *Radioengineering*, **23**, 914-921.

[19] Pushkar, K.L., Bhaskar, D.R. and Prasad, D. (2013) A New MISO-Type Voltage-Mode Universal Biquad Using Single VD-DIBA. *ISRN Electronics*, **2013**, 1-5.

[20] Pushkar, K.L., Bhaskar, D.R. and Prasad, D. (2013) Voltage-Mode Universal Biquad Filter Employing Single VD-DIBA. *Circuits and Systems*, **4**, 44-48. http://dx.doi.org/10.4236/cs.2013.41008

[21] Pushkar, K.L., Bhaskar, D.R. and Prasad, D. (2013) Single-Resistance-Controlled Sinusoidal Oscillator Using Single VD-DIBA. *Active and Passive Electronic Components*, **2013**, 1-5. http://dx.doi.org/10.1155/2013/971936

[22] Bajer, J., Vavra, J. and Biolek, D. (2014) Voltage-Mode Quadrature Oscillator Using VD-DIBA Active Elements. *IEEE Asia Pacific Conference on Circuits and Systems* (*APCCAS*), **4**, 197-200. http://dx.doi.org/10.1109/apccas.2014.7032755

[23] Prasad, D., Bhaskar, D.R. and Pushkar, K.L. (2013) Electronically Controllable Sinusoidal Oscillator Employing CMOS VD-DIBAs. *ISRN Electronics*, **2013**, 1-6.

[24] Bhaskar, D.R., Prasad, D. and. Pushkar, K.L. (2013) Fully Uncoupled Electronically Controllable Sinusoidal Oscillator Employing VD-DIBAs. *Circuits and Systems*, **4**, 264-268. http://dx.doi.org/10.4236/cs.2013.43035

[25] Prasad, D., Bhaskar, D.R. and Pushkar, K.L. (2011) Realization of New Electronically Controllable Grounded and Floating Simulated Inductance Circuits Using Voltage Differencing Differential Input Buffered Amplifiers. *Active and Passive Electronic Components*, **2011**, 1-8.

[26] Bhaskar, D.R., Prasad, D. and Pushkar, K.L. (2013) Electronically-Controllable Grounded-Capacitor-Based Grounded and Floating Inductance Simulated Circuits Using VD-DIBAs. *Circuits and Systems*, **4**, 422-430. http://dx.doi.org/10.4236/cs.2013.45055