

Modeling and Analysis of Variable Frequency Inverted Sine PWM Technique for a Hybrid Cascaded Multilevel Inverter

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Abstract

In cascaded H-bridge multilevel inverter, a variable frequency inverted sine PWM technique is modeled for hybrid electric vehicles. It has a particular advantage of increasing power which is achieved using series connection of H-bridge and also this topology is capable to produce superior spectral quality with considerable improvement of fundamental voltage. The variable frequency inverted sine PWM technique produces lesser torque ripple and enhances the fundamental output voltage mainly at lower modulation index ranges. The topologies of multilevel inverter are flying capacitor, diode clamped and cascaded inverter. In the paper, we will discuss about the cascaded multilevel inverter based on inverted sine PWM technique. The two switching strategies widely used to control multilevel inverters are constant frequency inverted sine PWM (CF-ISPWM) and variable frequency inverted sine PWM (VF-ISPWM). This implies that switch utilization substantially reduces 32.35% of the constant frequency inverted sine PWM switching technique. The performance of the technique is validated in terms of Total Harmonic Distortion (THD) and Torque ripple which significantly reduces when compared to constant frequency ISPWM. The analysis of conventional triangular PWM inverter and inverted sine PWM inverter using constant and variable switching scheme is done in MATLAB Simulink and verified experimentally by FPGA Spartan **3E processor.**

Keywords

Cascaded Multilevel Inverter, Constant Frequency Inverted Sine PWM, Variable Frequency Inverted Sine PWM, Total Harmonic Distortion

1. Introduction

Power Electronics based inverters are widely used in many industrial, aerospace and military applications because of their incredible concert on control capability and energy saving. Multi Level Inverter (MLI) is an attractive topology for high voltage DC-AC conversion. The reliability of power electronics system is directly related to the security of motor drive systems. The function of a multilevel inverter is to synthesize a desired staircase output waveform from several levels of dc input voltages that can be batteries, fuel cells, etc. [1] [2]. However, the topologies of multilevel inverter have several advantages such as better output quality, good electromagnetic compatibility, lesser number of sources, low switching losses, high efficiency capability to operate at high voltage and lower voltage stress on semiconductor device [3] [4]. Cascaded H-bridge topology significantly reduces the switches and harmonic content as the number of voltage levels increases more than other topologies. It also improves the reliability of MLIs by reducing the number of dc sources. It requires two unequal dc sources for producing nine-level output [5] [6]. Generally, (m - 1) carriers are needed to produce m-level output. Normally, each phase of cascaded multilevel inverter requires "*n*" dc sources for 2n + 1 level. The cascaded MLI is favorable for high power applications due to its modular structures. The unbalance problem of the dc link voltage does not occur. The main advantage of these topologies is that the rating of switching devices is highly reduced to the rating of each cell [7] [8].

Hussein Ashram M G, Fathi S H and Gharehpetian B have suggested selecting the suitable power semiconductor devices for asymmetric multi-level inverter which is very reliable and safe [9], so that the IGBT device is selected for this work. Jeevananthan S, Nandhakumar R and Dananjayan have introduced inverted sine carrier for fundamental strengthening in PWM inverters and FPGA based implementations [10], but it is not suitable for variable frequency ISPWM. Thomas A. Lipo has introduced an improved weighted total harmonic distortion for induction motor [11], and it is superior to the THD which predicts the distortion in the current and consequent supplementary losses. Magdun O. Binder has introduced the calculation of high frequency induction machine parameters [12], and their influence is towards the stator current. Even though these approaches are well suitable for the sinusoidal PWM method, it is difficult to apply for inverted sine PWM method. The most popular technique is the variable frequency ISPWM method which is implemented in this paper. Conventionally, triangular wave is used as a carrier in PD-PWM method, whereas inverted sine carrier waves are replaced in our proposed PD-PWM technique. A high switching frequency inverted sine carrier wave is compared with the reference sine wave, which generates pulses when the amplitude of the reference sine wave is greater than the inverted sine carrier wave [10]. The constant frequency carrier based PWM increases the switch utilization in multilevel inverters. Thus, the variable frequency carrier based PWM is proposed to balance the switching duty among the various levels in inverters [13]. The proposed strategy is employed in single-phase RL Load. Using this technique load voltage is obtained for hybrid cascaded inverter. The efficiency of the proposed method is measured based on the evaluation metrics *i.e.*, THD and Switch utilization in percentage.

The paper is organized as follows: Section 2 introduces hybrid cascaded multilevel inverter and Section 3 explains variable frequency inverted sine PWM technique. Simulation results and Experimental results have been presented in Sections 4 and 5 respectively. Finally Section 6 concludes this paper.

2. Hybrid Cascaded Multilevel Inverter

Multiple dc sources are required for many applications which increases the cable length and this could lead to voltage unbalance among the dc sources [14]. To reduce the number of required dc sources in cascaded multilevel inverter, an asymmetric topology is proposed which uses only two dc sources to generate nine-level output as shown in **Figure 1**. The optimal asymmetry has been achieved by voltage sources which are proportionally scaled to the two- or three-H bridge. The number of levels in phase voltage obtains as follows.

$$m = 3^{n} \text{ if } V_{dci} = 3^{(i-1)} V_{dc} \quad i = 1, 2, \cdots, n$$
(1)

where, n is the number of H-bridge cells per phase.

The hybrid cascaded multilevel inverter consists of two H-Bridges. The first H-Bridge H₁ consists of dc source $1V_{dc}$ whereas the second H-Bridge H₂ consists of dc source $3V_{dc}$ is as shown. Each dc source is connected to a single phase inverter. Each inverter level can generate three different voltage outputs $+V_{dc}$, 0 and $-V_{dc}$ by various combinations of the four switches S₁, S₂, S₃ and S₄. When switches S₁ and S₄ are ON, the output is $+V_{dc}$, when either pair S₁ and S₂ or S₃ and S₄ are ON, the output is



Figure 1. Hybrid cascaded MLI with unequal dc sources.

0 [15]. The output voltage H₁ can be made equal to $-1V_{dc}$, 0, or $1V_{dc}$, similarly the output voltage of H₂ can be made equal to $-3V_{dc}$, 0, or $3V_{dc}$ by opening and closing its switches appropriately. Therefore, the output voltage of the inverter have the values $-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0, $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc} can be designed, as shown in **Figure 2**. The output voltage of the first H-bridge is represented by V_1 and the second H-bridge is represented by V_2 . The output voltage is $V = V_1 + V_2$. **Table 1** shows the conduction sequence of each switch for hybrid multilevel inverter at different voltage levels.

3. Variable Frequency Inverted Sine PWM Technique

The proposed control strategy replaces triangular carrier waveform by variable frequency inverted sine wave so it is known as Inverted sine PWM techniques. The main objective of the proposed method deals THD minimization and switch utilization in a considerable manner for the progress of efficiency factors in MLIs. The proposed PWM strategy replaces the conventional constant frequency carrier waveform by variable frequency inverted sine wave [16]. In constant frequency carrier waveform there is marginal boost in the magnitude at lower order harmonics and unbalanced switch utilization [17]. This can be overcome by implementing variable frequency inverted sine carrier signals. The inverted sine PWM has got better spectral quality and higher fundamental voltage compared to the triangular based PWM. This control strategy uses a high frequency inverted sine carrier which helps to maximize the output voltage for a given modulation index [10] [18].

The significance of ISPWM methods are:

1) Spectral quality is better and fundamental component is higher when compared to the conventional sinusoidal PWM.

2) The ISCPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges.

3) Reduction in THD.

4) Low switching losses.

5) Due to improvement of THD in the lower range of modulation index, this is applicable for low speed drive application.

Total Harmonic Distortion (THD) decreases and switching losses increases with increase in switching fre-



Figure 2. Output voltage of bridges. (a) Output voltage for first bridge of MLI; (b) Output voltage for second bridge of MLI; (c) Output voltage of hybrid MLI.

Table 1. Switching	able 1. Switching states of hybrid cascaded MLI.								
Voltage	\mathbf{S}_1	S_2	S ₃	S_4	S ₅	S ₆	S ₇	S_8	
$4V_{dc}$	On	Off	Off	On	On	Off	Off	On	
$3V_{dc}$	On	On	Off	Off	On	Off	Off	On	
$2V_{dc}$	Off	On	On	Off	On	Off	Off	On	
$1V_{dc}$	On	Off	Off	On	On	On	Off	Off	
$-1V_{dc}$	Off	On	On	Off	Off	Off	On	On	
$-2V_{dc}$	On	Off	Off	On	Off	On	On	Off	
$-3V_{dc}$	Off	Off	On	On	Off	On	On	Off	
$-4V_{dc}$	Off	On	On	Off	Off	On	On	Off	

quency and switching loss. The graph is plotted with THD, switching losses and switching frequency to obtain a low value of THD and switching losses. The optimum frequency is found to be 3950 Hz and the corresponding THD and switching loss is found from the graph shown in **Figure 3**. VFISPWM method combines the advantage of variable frequency carrier signals and inverted sine. It has an enhanced fundamental voltage and minimizes the switch utilization between the various levels in inverters. The control signals have been generate by comparing the sinusoidal reference signal with a variable frequency inverted sine carrier signal. The carrier frequencies are selected such that the number of switching in each bands are equal. The frequency ratio for each band should be set properly in order to balance the switching action for all levels [13] [19] as explained in **Figure 4**.

In Figure 3(b), the modulating wave [20] is defined as

$$V(t) = \sin\theta \tag{2}$$

where θ = Switching angle.

The calculation of the slope values for the four bands is shown below:

$$\theta_1 = \operatorname{Sin}^{-1}(0) = 0 \text{ radians}$$
(3)

$$\theta_2 = \operatorname{Sin}^{-1}(1/4) = 0.2526 \text{ radians}$$
 (4)

$$\theta_3 = \operatorname{Sin}^{-1}(2/4) = 0.5235 \text{ radians}$$
 (5)

$$\theta_4 = \operatorname{Sin}^{-1}(3/4) = 0.8480 \text{ radians}$$
 (6)

$$\theta_5 = \operatorname{Sin}^{-1}(1) = 1.5707 \text{ radians}$$
 (7)

Slope of
$$C1 = 0.9897$$
 (8)

Slope of
$$C2 = 0.9228$$
 (9)

Slope of
$$C3 = 0.7704$$
 (10)

Slope of
$$C4 = 0.3459$$
 (11)

Frequency of
$$C1 = 3950 \text{ Hz}$$
 (12)

Frequency of
$$C2 = 3645 \text{ Hz}$$
 (13)

- Frequency of C3 = 3043 Hz (14)
- Frequency of C4 = 1366 Hz (15)



Figure 3. (a) Optimum frequency calculation for variable frequency PWM technique; (b) Reference modulating wave—four bands for different carrier frequency.



Figure 4. Carrier and reference waveforms of VF-ISPWM

4. Simulation Result

In our proposed method, the strategy spotlighted on Phase Disposition (PD) based inverted sine PWM (ISPWM) for nine-level inverter. The parameters chosen for simulation using the proposed PWM technique is as shown in **Table 2**. Thus the proposed VF-ISPWM technique is proved the minimized THD and Switch utilization is significantly reduces 32.35% of the CF-ISPWM switching technique as depicted in **Table 3**. The comparative analysis over conventional PWM techniques is shown in **Table 4**.

From the **Table 3** and **Table 4** it is observed that variable frequency inverted sine PWM has a better spectral quality when compare to other PWM methods. The hybrid cascaded inverter is simulated for different modulation index and carrier frequency values using MATLAB/SIMULINK. Figure 5 show the load current waveform. Figure 6 shows the load current spectrum. Figure 7 shows the load voltage waveform and Figure 8 shows the load voltage spectrum of proposed methods for ma = 0.9 and V_{dc} = 300 V. As we shown, the proposed VFISPWM technique always claims lower THD than CFISPWM technique and the Load voltage waveform shows that the top and bottom levels of VFISPWM technique has less number of switching compared to the CF-ISPWM technique.

Figure 9 details the comparison of THD (%) vs. Modulation Index (ma) graphically. These results show that the VFISPWM method gives harmonic reduction for individual harmonic. Hence, the VF-ISPWM scheme is more favorable than the CF-ISPWM technique for hybrid asymmetric multilevel inverter.

From the above results, it is also observed that VFISPWM gives an enhanced fundamental voltage and reduced total harmonic distortion. To verify the robustness of the proposed scheme, a simulation model for a single phase hybrid cascaded MLI with Induction motor load is implemented. The motor specifications are revealed in Table 5. To prove the performance of the single phase asymmetric MLI with motor load simulation is experimented using SIMULINK block set is as shown in Figure 10 and the simulation results are verified. Figure 11 shows the stator current of 1ϕ induction motor.

The rotor speed for 1ϕ induction motor is shown in **Figure 12**. From the observation the rotor speed is always less than synchronous speed, so this machine is called as Asynchronous machine. The stator winding is wound for certain definite number of poles which is excited by a single phase a.c. supply so that stator produces the magnetic field which creates the effect of number of poles for which stator winding is wound, its decides the synchronous speed of the motor. The synchronous speed is denoted as N_s . The relation is given by [21],



-400 -500 0 0.005 0.01 0.015 0.02 0.025 0.03 0.035 0.04 Time (ms) (b)

Figure 7. Load voltage waveforms. (a) VF-ISPWM; (b) CF-ISPWM.



Figure 8. Output load voltage spectrum. (a) VF-ISPWM; (b) CF-ISPWM.



Figure 9. Variation of THD with modulation index for Constant Frequency (CF) and Variable Frequency (VF) ISPWM.

Table 2. P		

S. No	Parameters	Values		
1	Main DC Source Voltage (V _{dc})	300 V		
2	Modulation Index (ma) 0.9			
3	New Carrier Frequency	3950 Hz, 3645 Hz, 3043 Hz, & 1366 Hz		
4	Frequency Modulation Ratio (mf)	mf1 = 79, mf2 = 73, mf3 = 61 & mf4 = 27		
5	RL Load	$R = 10 \Omega$; $L = 0.024 mH$		
6	Rated Output Frequency	50 HZ		
7	Reference Voltage	300 V		

Table 3. Switching actions for the PWM techniques.

Parameter	CFISPWM	VFISPWM
Nsw	68	46
V-THD	18.27%	10.02 %
I-THD	3.07 %	2.90 %

Table 4. Comparative analysis over conventional PWM techniques.

Demonstern	Constan	t Frequency	Variable Frequency		
Parameter	Triangular PWM	Inverted Sine PWM	Triangular PWM	Inverted Sine PWM	
V-THD	12.76%	18.27%	8.69%	10.02%	
I-THD	2.93%	3.07%	2.93%	2.90%	



Figure 10. Simulation circuit for 1ϕ asymmetric hybrid cascaded MLI with induction motor.



Figure 11. Stator current for 1ϕ induction motor.

 Table 5. Motor specifications.

Parameters	Values
Rating	186.5 W, 110 V, 50 Hz, 1440 rpm
Stator Resistance (Rs)	2.02 Ω
Rotor Resistance (Rr)	4.12 Ω
Inductance	Ls = 0.278 H, Lm = 0.177 H
Moment of Inertia	0.0146 J
Pole Pairs	2



Figure 12. Rotor speed for 1ϕ induction motor.

$$N_s = \frac{120f}{P}$$

where N_s = synchronous speed [rpm]; f = frequency of the source [Hz]; p = number of poles. The rotor turn at slightly less than synchronous speed and the full-load slip is typically 3 percent to 5 percent for fractional horsepower motors [22].

The electromagnetic torque and the stator flux for a 1ϕ induction motor are shown in Figure 13. The starting torque can be increased in induction motor by increasing the rotor resistance. Torque is the turning or twisting force through a radius and the units is rated in Nm. The torque developed by asynchronous induction motors varies with the speed of the motor when accelerates from zero speed to maximum operating speed. A high starting torque is more significant for application where hard to start such as positive displacement pumps, cranes. A lower starting torque can be established in applications such as centrifugal fans or a pump where the start loads is close to zero or low. The pull-up torque is the minimum torque residential by the electrical motor when it runs from zero speed to full load speed. Breakdown torque is the highest torque existing before the torque decreases when the machine continues to accelerate to the working conditions [23].

From the speed and torque curves, it is seen that rated speed quickly achieved within 0.2 ms and the torque is quickly settled at 0.25 ms. Therefore the proposed hybrid multilevel inverter can be used for variable speed drive applications which can be obtained by varying the frequency of multilevel inverter. The harmonics in induction motor sometimes exhibit to run stably as low as 1/7 of the synchronous speed. This could be avoided by reducing the harmonics which are shown in **Figure 14** and **Figure 15**. The total harmonic distortion is a measure of proximity in shape between a waveform and its fundamental component, the expression for THD is [8] [24].

THD =
$$\frac{1}{(V_0)_1} \sqrt{\sum_{3.5.7}^{\infty} (V_0)_n^2}$$

where $(V_0)_n$ is the rms value of harmonic component and $(V_0)_1$ is the rms value of fundamental component.

The number of possible output voltage levels is twice the number of dc sources so the complexity in the cir-



Figure 13. Electromagnetic torque and stator flux for 1ϕ induction motor.



Figure 14. (a) FFT analysis of load current for VFISPWM; (b) FFT analysis of load voltage for VFISPWM.



Figure 15. THD of phase voltage for different ISPWM methods.

cuits for higher order levels with high power loads can be reduced and the series of H-bridge makes for modularized layout and packaging. This will make the manufacturing process to be done in quickly and cheaply. This structure is favorable for high power application since its produces higher voltage at higher modulation frequencies with low switching frequency. The multilevel inverter can be implementing for Hybrid Electric Vehicles (HEV) and Electric Vehicles (EV). The HEV combines a conventional IC engine, battery pack and an electric motor whereas the EV includes rechargeable batteries and an electric motor. The multilevel inverter that drives the electric motor is an input device for HEV and EV [25] [26].

Moreover, the performance parameters measured for evaluating the proposed modulation strategy are: Crest factor, Distortion factor, WTHD and HSF.

4.1. Crest Factor (CF)

Crest factor is a measure of a waveform, such as alternating current or sound, showing the ratio of peak value to average value. Crest factor value 1 indicates no peaks, but higher crest factors indicate peaks.

$$CF = \frac{V_{\text{peak}}}{V_{\text{rms}}}$$

where, V_{peak} is the Peak Voltage and V_{rms} is the R.M.S Voltage.

4.2. Distortion Factor (DF)

The distortion factor is the result from a mathematical equation which resembles the geometrical means. The intensity of the nonlinear distortions is measured.

$$\mathbf{DF} = \frac{1}{V_1} \left[\sum_{n=2,3}^{\infty} \left(\frac{V_n}{n^2} \right)^2 \right]^{1/2}$$

where, V_1 is the Fundamental voltage, V_n is the total harmonics voltage and n is the order of the harmonics.

4.3. Weighted THD (WTHD)

The weighted total harmonic distortion (WTHD) is a commonly used to evaluate the quality of pulse width modulation (PWM) inverter waveforms. The WTHD weights the voltage harmonics is inversely with its frequency. Whereas this is tolerable for some inductor type loads, the commonly employed induction motor load has significant effects resulting from eddy currents in the rotor bars not included in the WTHD [11].

WTHD =
$$\frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{V_n}{n}\right)^2}}{V_1}$$

4.4. Harmonic Spread Factor (HSF)

Harmonic Spread Factor is the deciding factor to indicate noise generation in the motor. The harmonic spread factor is calculated for evaluating the quality of voltage spectrum of inverters.

$$\text{HSF} = \sqrt{\frac{1}{N} \sum_{j=2}^{N} \left(H_j - H_0 \right)^2}$$

where, H_i is the value of j_{th} harmonic and H_0 is the average value of all N Harmonics.

From Table 6, it is found that the proposed modulation technique normalizes reduced THD, WTHD and distortion factor.

Moreover, with variable frequency, enhanced fundamental output is obtained. It has to be emphasized that less torque ripple for variable frequency PWM technique leads to better stability operation with minimum mechanical noise.

able 6. Performance parameter of hybrid MLI.							
S. No	Parameters	CF ISPWM	VF ISPWM				
1	$V_{ m rms}$ (V)	251.1	255.1				
2	$V_{ m peak}$ (V)	355.1	360.7				
3	Crest Factor (CF)	1.414	1.414				
4	Distortion Factor (DF)	0.017	0.0055				
5	Weighted THD (WTHD)	0.257	0.083				
6	Harmonic Spread Factor (HSF)	3.191	2.247				
7	Torque Ripple (%)	17.9	7.9				

5. Experimental Result

To validate the single-phase asymmetric hybrid cascaded H-bridge multilevel inverter, a prototype module is built using CT60AM18F smart power module (SPM) as the switching devices and is experimented as shown in **Figure 16**. SPARTAN-3E FPGA processor is used to implement the gating pattern that associates and evaluates with other modules, hybrid MLI setup (optocoupler, driver & power circuit) and load configuration.

The inverter was first controlled by using constant frequency ISPWM with the following parameters: ma = 0.9 and mf = 79. The prototype inverter was tested using the proposed VFISPWM with different carrier frequencies which balances the switching actions and gives a lower value of THD compared to the CFISPWM. Hardware set-up for Single phase power circuit with optocoupler is exposed in **Figure 16(a)** and the experimental setup for the asymmetric MLI is shown in **Figure 16(b)**.

The specifications for semiconductor device are: Part Number: CT60AM-18F, Voltage rating = 900 V and Current rating = 60 A. Figure 17 shows the block diagram of proposed system.

PWM generators incorporated within microcontrollers are not normally flexible enough to generate switching pulse, so that Field Programmable Gate Array (FPGA) based controller is employed. The pulse produced by FPGA processor is transmitted through an optocoupler to the multilevel inverter. The core processor of the system is a Xilinx FPGA, Spartan 3E programmed through a Xilinx EEPROM. The FPGA program is downloaded from Personal Computer through a parallel cable to the EEPROM using master serial mode and the stored program in the electrically erasable programmable ROM (EEPROM) is reloaded to the FPGA once it is reset [27]. Figure 18 shows the load voltage and load current waveform.

The proposed strategy is employed for single phase RL load which have the value of R = 10 ohms and L = 0.024 mH. The inductance value is small, so that the load voltage and load current waveforms are identical. The simulation is carried out for the motor load in order to calculate the performance of the MLI with Variable frequency ISPWM. This will be helpful to design the hardware for induction motor load.

From the above **Table 7**, it is seen that variable frequency ISPWM reduces the harmonics for both simulation and experimental work when compare to constant frequency inverted sine PWM. **Figure 19** shows experimental results with power quality analyzer. The variable frequency inverted sine PWM gives reduced harmonics as **VTHD = 4.45% & ITHD = 5.95%** where as constant frequency inverted sine PWM gives **VTHD = 6.28% & ITHD = 6.25%**.

Insulated Gate Bipolar Transistor (IGBT) is a very popular device among power semiconductor due to its easy switching and handles high level of power demand by Hybrid Electric Vehicles (HEV) motor drives. In this work, Cascaded H-Bridge Multilevel Inverter can be interfaced with electric drives of HEVs because of following features.

1) When compare to diode clamped and flying capacitor MLI, the number of components is less.

2) It is suitable for high current and low voltage rating electric drives which are needed for Hybrid Electric Vehicles.

3) Cascaded H-Bridge Multilevel Inverter can be switched at low frequency, so that noise can be suppressed which is comfortable for driving HEVs [25].

The three single-phase multilevel inverter are connected in parallel to add up the voltage. The output of the three single phase inverter needs to be synchronized with separation of 120 degree between each phase. So that we can implement for three phase circuit.



Figure 16. (a) Hardware setup; (b) Experimental setup; (c) CRO nine-level output.



Figure 17. Block diagram of the proposed system.



Figure 18. Experimental load voltage and load current waveforms.

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		Order			Orden		h -16 F0/ 1	
fPLL1:U1	1 39.821 Hz	Order Total	U1 [V] 10.825	hdf [%]	Order	U1 [V]	hdf [%]	Element 1 HRM1 U1 10V
fPLL2:11		10tai 1	10.825	99.900	dc	0.031	0.288	11 1A
		3	0.134	1.234	2	0.057	0.529	Sync Src: 11
Urms1	11.005 V	5	0.069	0.642	4	0.025	0.234	Element 2 HRM1
Irms1	0.0000 A	7	0.253	2.333	8	0.034	0.313	U2 15V I2, 1A
P1	0.000 W	9	0.047	0.433	10	0.026	0.240	Sync Src: 12
S1	0.000 VA	11	0.143	1.325	12	0.038	0.353	Element 3 HRM1
Q1	0.000 var	13	0.148	1.367	14	0.007	0.065	US 60V IS 1A
λ1	Error	15	0.046	0.428	16	0.018	0.167	Sync Src: 13
Φ1	Error	17	0.126	1.166	18	0.010	0.107	Element 4 HRM1
L. L.		19	0.163	1.501	20	0.015	0.120	
Uthd1	4.455 %	21	0.122	1.129	22	0.012	0.107	U4 60V 4 5A Sync Src: 4
lthd1	5.952 %	23	0.052	0.482	24	0.033	0.303	
Pthd1	8.025 %	25	0.014	0.132	26	0.019	0.177	Element 5 HRM1
Uthf1	3.676 %	27	0.012	0.115	28	0.018	0.168	U5 60V I5 5A
lthf1	9.170 %	29	0.009	0.085	30	0.012	0.115	Sync Src: 15
Utif1	0 F	31	0.024	0.221	32	0.017	0.161	Element 6 HRM1
ltif1	0 F	33	0.034	0.312	34	0.023	0.213	U6 30V 6 5A
hvf1	1.491 %	35	0.016	0.148	36	0.017	0.154	Sync Src: 🔟
hcf1	1.325 %	37	0.061	0.564	38	0.009	0.082	
Kfact1	2.0954 k	39	0.035	0.326	40	0.007	0.065	
	1/11				-	PA	GE <mark>-</mark> 1/13	
				(a)				
		Order	U1 [V]	hdf [%]	Order	U1 [V]	hdf [%]	Element 1 HRM1
fPLL1:U ²	1 44.822 Hz	Total	10.608		dc			
fPLL2:11		1	10.587	99.802	2	<u>-0.003</u> 0.067	-0.031 0.632	U1 10V 10 10mA Sync Src: 11
		3	0.483	4.553	4	0.016	0.032	
Urms1	10.797 V	5	0.275	2.588	6	0.017	0.140	Element 2 HRM1
Irms1	10.606 mA	7	0.066	0.619	8	0.021	0.201	U2 15V I2 1A
P1	114.50 mW	9	0.153	1.447	10	0.006	0.059	Sync Src: 12
S1	114.51 mVA	11	0.025	0.236	12	0.008	0.071	Element 3 HRM1
Q1	1.02 mvar	13	0.072	0.674	14	0.011	0.107	U3 60V I3 1A
λ1	1.0000	15	0.121	1.138	16	0.005	0.048	Sync Src: 13
Φ1	G0.51 °	17	0.044	0.418	18	0.020	0.190	Element 4 HRM1
		19	0.146	1.373	20	0.009	0.087	U4 60V 14 5A
Uthd1	6.282 %	21	0.125	1.183	22	0.016	0.149	14 5A Sync Src: 14
Ithd1	6.255 %	23	0.062	0.582	24	0.004	0.038	Element 5 HRM1
Pthd1	0.393 %	25	0.046	0.438	26	0.021	0.194	
Uthf1	4.073 %	27	0.053	0.502	28	0.013	0.127	U5 60V 15 5A
lthf1	4.065 %	29	0.053	0.504	30	0.034	0.319	Sync Src: 15
		31	0.045	0.425	32	0.049	0.464	Element 6 HRM1
Utif1	0 F	<u> </u>				0.000	0.070	U6 30V 6 5A
	0 F 0 F	33	0.053	0.504	34	0.008	0.073	16 5A
Utif1 Itif1 hvf1		33 35		0.504 0.422	34 36	0.008	0.073	Sync Src: 6
Utif1 Itif1	0 F	33 35 37	0.053					
Utif1 Itif1 hvf1	0 F 3.027 %	33 35	0.053 0.045	0.422	36	0.011	0.106	
Utif1 Itif1 hvf1 hcf1	0 F 3.027 % 3.009 % 2.0145	33 35 37	0.053 0.045 0.015	0.422 0.138	36 38	0.011 0.011 0.016	0.106 0.104	

(b)

Figure 19. THD values of load voltage and load current measured using PQ analyzer. (a) VF-ISPWM; (b) CF-ISPWM.

Table 7. Validation of experimental and simulated results.								
Parameter	CFISI	PWM	VFISPWM					
Parameter	V-THD	I-THD	V-THD	I-THD				
Simulation Result	18.27%	3.07%	10.02%	2.90%				
Experimental Result	6.28%	6.25%	4.45%	5.95%				

6. Conclusion

Thus the simulation and experimental results demonstrated the ability of the proposed methodology to effectively be used to increase the performances of the MLIs. A comparative evaluation between CFISPWM & VFISPWM methods has been presented in terms of output voltage quality, power circuitry complexity and THD. From this observation VFISPWM technique provides an enhanced fundamental voltage and reduced THD compared to other conventional strategies. To overcome the marginal boost in the magnitude of lower order harmonics and unbalanced switch utilization, variable frequency inverted sine carrier signals are employed. Now, it is proved that the VFISPWM method gives a better performance and THD for a chosen modulation index. Further, the proposed MLI with reduced number of switches can also be employed for electric vehicle applications.

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