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Analysis of Reduced Switch Topology Multilevel Inverter with Different Pulse Width Modulation Technique and Its Application with DSTATCOM

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Abstract

Multilevel inverter has played a vital role in medium and high power applications in the recent years. In this paper, Reduced Switch Count Multi Level Inverter structure (RSCMLI) topology is presented with different pulse width modulation techniques. The harmonic level analysis is carried out for the reduced switch count multilevel inverter with the different PWM technique such as with Alternate Phase Opposition Disposition (APOD) method, In Phase Disposition (IPD) method and multi reference pulse width modulation method for five level, seven level , nine level and eleven level inverter. The simulation results are compared with the cascaded H Bridge Multi Level Inverter (CHBMLI). The nine level RSCMLI inverter with APOD method is used for the Distribution Static Synchronous Compensator (DSTATCOM) application in the nonlinear load connected system for power factor improvement. The result shows that the harmonic level and the number of switches required for RSCMLI is reduced compared to CHBMLI. RSCMLI employed in DSTATCOM improves the power factor and harmonic level of the system when it is connected to the nonlinear load.

Keywords

Reduced Switch Count Multilevel Inverter, PWM Method, Harmonic Level, DSTATCOM

1. Introduction

Multilevel inverter is used in many applications in industries and in other fields which suits for high power and

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high voltage applications. The two level inverter is used in the low voltage and low power applications. For medium and high voltage application with two level inverter, the voltage stress on each power electronic switch and its switching losses will be more and harmonic level will be increased, it also requires large filter size. Multilevel inverter overcomes this problem and the voltage level can be increased to a required level which suits for medium to high voltage and high power application. Multilevel inverter topologies are classified into three types Diode Clamped Multilevel Inverter, Flying Capacitor Multilevel Inverter, Cascaded H Bridge Multilevel Inverter. Among these Cascaded H Bridge MLI is simple in structure and requires fewer components. As the level goes on increasing the semiconductor device required, it will be more and the structure becomes large. Multilevel inverter with less switch count is the interest of the researchers in the recent years where it can generate required level of output voltage with minimum switch count. There are different topologies for reduced switch count MLI which has been listed in [1]-[6]. Nasrudin *et al*. [1] presented a single phase seven level reduced switch count multilevel inverter for grid connected photovoltaic system. Reduced Switch Count MLI with APOD PWM method for MLI fed motor drive is discussed in [2]. Rajan *et al*, [3] discussed a new topology of reduced switch structure multilevel inverter with different PWM techniques and the harmonic level is compared for different modulation index. Nine types of reduced switch topologies are discussed [4] based on its structure, required number of switches and the comparison have made among the topologies to suit for an application and in [6] analysis of multilevel inverter topologies, its control and application has been reviewed.

Multilevel inverter topologies are used in the application of custom power electronic device to mitigate power quality issues. Distribution Static Synchronous Compensator (DSTATCOM) is a device used to mitigate the power quality issues like voltage sag, swell, power factor improvement and reactive power compensation. MLI is used in the voltage source inverter part of the DSTATCOM [7]-[10] which generally uses two level inverter. There are different control techniques for the DSTATCOM controller, the other control techniques are based on SRF theory, IRP theory [11] and fuzzy logic based controller [12], artificial intelligence based controller is discussed in [13] [14].

From [1], RSCMLI topology is analysed for five level, seven level, nine level and eleven level MLI. The topology consists of conventional H bridge unit with bidirectional switch structure. The harmonic analysis is carried out for this structure for five, seven, nine and eleven level with the different PWM method such as with the multireference PWM method and with multicarrier methodology [2] of APOD and IPD method with a rectified reference signal. The nine level RSCMLI with the multireference PWM technique from [1] is carried out and is presented in [15] and the VSI part of DSTATCOM for power factor improvement when connected to a nonlinear load system. In this paper the harmonic analysis is carried out for the RSCMLI structure with the above mentioned PWM techniques and is compared with the harmonic level of Cascaded H bridge MLI topology. The RSCMLI structure with minimal harmonic level is used in the voltage source inverter part of DSTATCOM for power factor improvement in the nonlinear load connected system. The simulation of the system and the results are analysed using MATLAB/Simulink software. The paper is organized as follows; In Section II DSTATCOM with system configuration is discussed, in section III RSCMLI structure and in section IV the PWM techniques are discussed in detail. In section V the simulation results are analysed for the system.

2. DSTATCOM with System Configuration

DSTATCOM is connected in shunt to the three phase supply of 415 V, 50 Hz system at the point of common coupling point (PCC) connected to a nonlinear load of rectifier unit with RC load. The DSTATCOM structure consists of a dc energy source connected to the voltage source inverter (VSI) part with the reduced switch count topology structure and is connected to the ac system with filter unit through coupling transformer. The RSCMLI structure of nine level is used in the VSI part of DSTATCOM. **Figure 1** shows the configuration of the DSTATCOM with the system. DSTATCOM is used in the nonlinear load connected system for power factor improvement and to reduce the harmonic level. The reduced switch count structure and PWM technique are discussed in the following section.

3. Reduced Switch Count Multilevel Inverter (RSCMLI) Structure

The reduced switch count multilevel inverter structure consists of a conventional H bridge unit with bidirectional switches in it to get the required voltage level with a single dc source and with voltage dividing capacitors. **Figure 2** shows the eleven level RSCMLI single phase structure of this topology. The RSCMLI structure for an

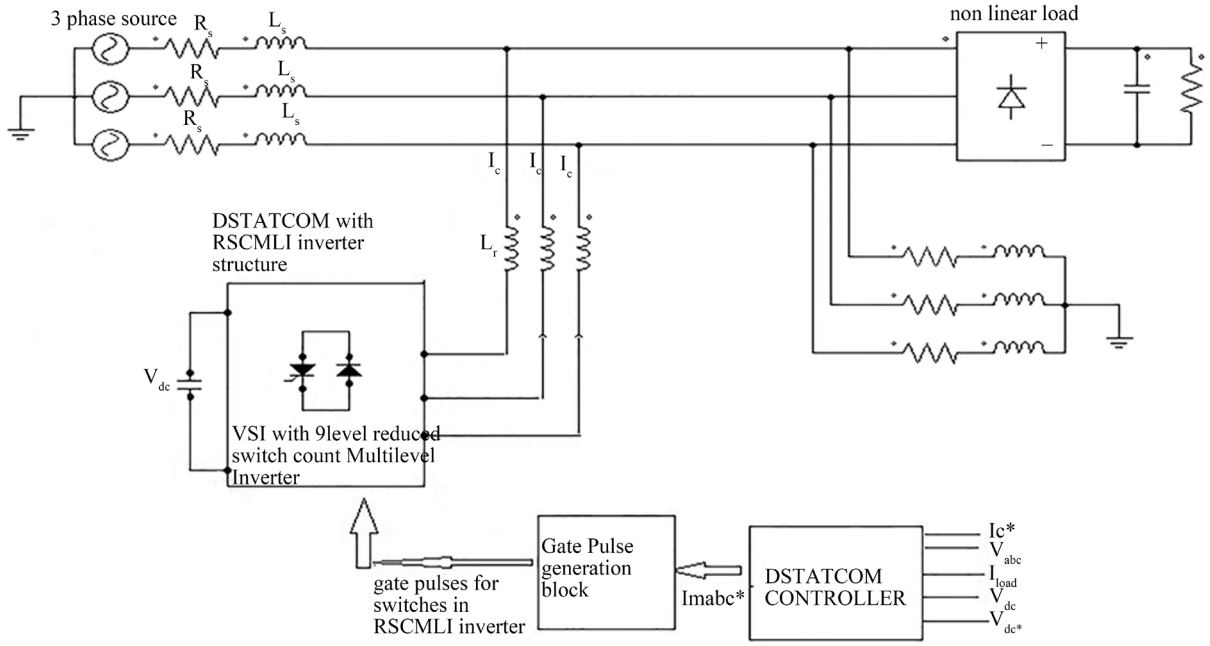


Figure 1. Block Diagram of the system with DSTATCOM.

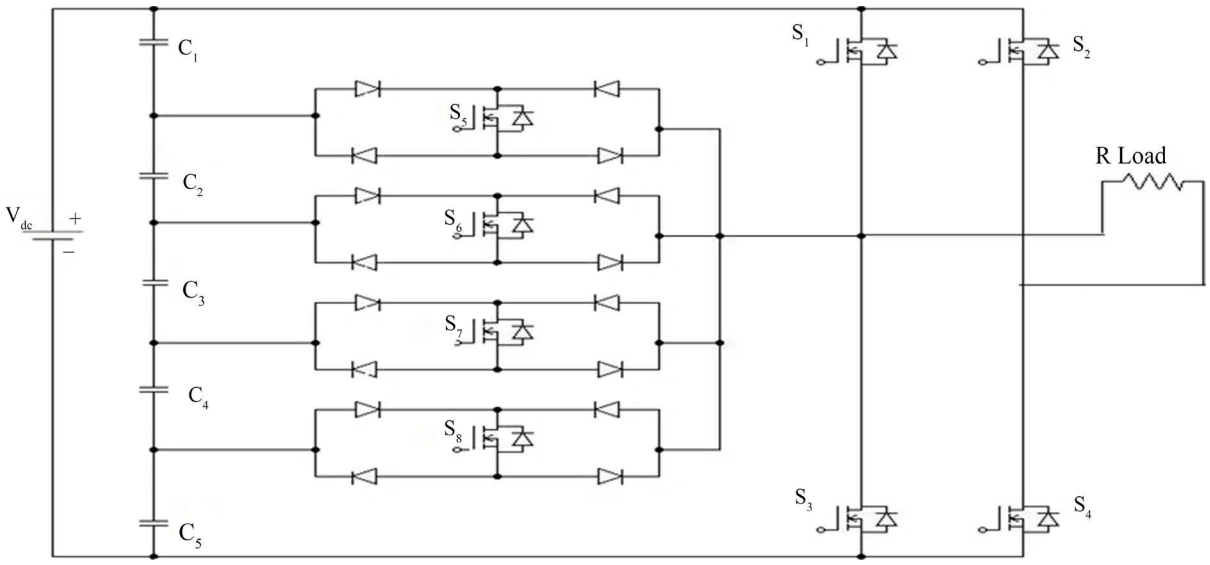


Figure 2. Single phase structure of eleven level Reduced Switch Count Multilevel (RSCMLI) Inverter.

N-level requires [((N − 1)/2) + 3] switches. **Figure 3** shows the three phase structure of nine level RSCMLI inverter. For five level inverter it has single H bridge unit with a bidirectional switch and has two voltage dividing capacitor. For seven level inverter it has single H bridge unit with two bidirectional switches and requires three voltage dividing capacitor with single dc source. For nine level inverter, it requires three bidirectional switches with single H bridge unit and with four voltage dividing capacitors. For eleven level inverter, it requires four bidirectional switches with single H bridge unit and requires five voltage dividing capacitors with single dc source. The required switches for five level will be five switches, for seven level it requires six switches, for nine level it requires seven switches and for eleven level it requires eight switches. Compared to the cascaded H Bridge MLI the number of switches required will be less for this RSCMLI inverter. For a single phase eleven level inverter of CHBMLI requires twenty switches with five separate dc sources and for the eleven level RSCMLI structure requires eight switches with single dc source and with five voltage dividing capacitor.

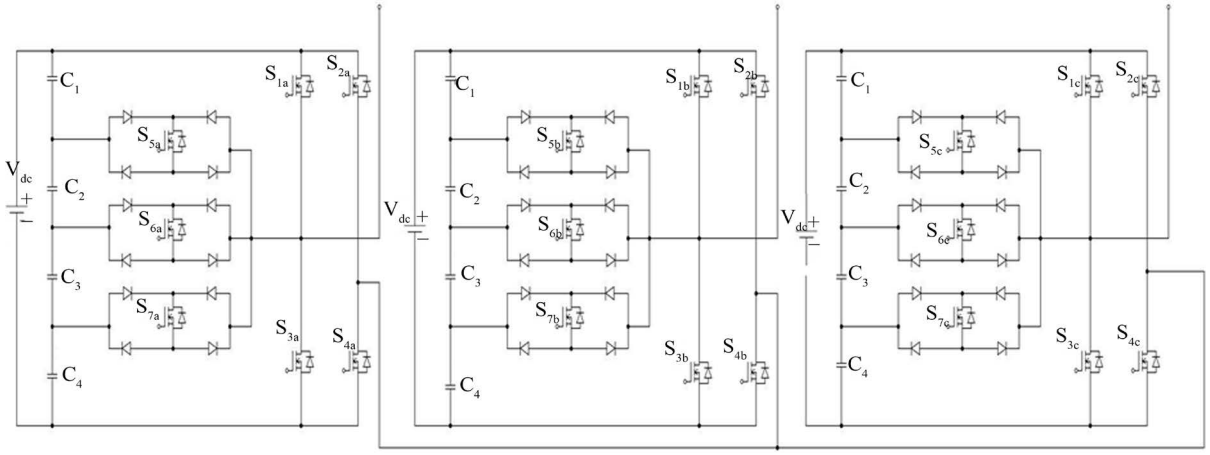


Figure 3. Three phase structure of nine level RSCMLI.

4. Pulse Width Modulation Technique for RSCMLI Inverter

The pulse width modulation technique is the key part in the multilevel inverter to trigger the switches at the proper instant and to get the required level of output voltage. In this paper the following PWM methods are used for the reduced switch count MLI in order to get the required level of output voltage and the harmonic analysis is carried for the RSCMLI with these PWM techniques. For this RSCMLI topology with the PWM techniques switches S2, S4 operates at fundamental frequency and other switches are operating at switching frequency.

4.1. Multicarrier Alternate Phase Opposition Disposition (APOD) PWM Method

In the Multicarrier Alternate Phase Opposition Disposition method [2] for an N level of inverter it requires (N − 1)/2 carrier signals and is placed above the zero axis and the carrier signals are alternatively opposite in phase as shown in **Figure 4** is compared with a rectified reference signal. The reference signal is operating at the fundamental frequency of 50 Hz and the carrier signals with switching frequency of 10 KHz. The modulation index is given by

$$m = V_m / (n * V_c) \tag{1}$$

where m is the modulation index, V_m is the magnitude of the reference signal, n is the number of carrier signals required for an N level and V_c is the magnitude of the single carrier signal. For 5 level inverter it requires two carrier signal, for 7 level inverter it requires three carrier signal, for 9 level inverter it requires four carrier signal, for eleven level inverter it requires five carrier signal. For the eleven level inverter the modulation index is calculated as $m = 4.5/(5 \times 1)=0.9$, where $V_m = 4.5$, $V_c = 1$, $n = 5$.

The reference signal is compared with the carrier signals to generate gate pulse for the switches and the output of the required level will be obtained. For the eleven level inverter, $V_{\text{carrier5}}(V_{c5})$ is compared with V_{ref} until V_{ref} exceeds the magnitude of V_{c5} then V_{ref} is compared with V_{c4} until V_{ref} exceeds the magnitude of V_{c4} then V_{ref} is compared with V_{c3} until V_{ref} exceeds the peak magnitude of V_{c3} then V_{ref} is compared with V_{c2} until V_{ref} exceeds the magnitude of V_{c2} then V_{ref} is compared with V_{c1} until it exceeds the magnitude of V_{c1} and then goes on. Switches S_2 and S_4 operates at the fundamental frequency and the remaining switches S_1, S_3, S_5, S_6, S_7 and S_8 operates at the switching frequency.

4.2. Multicarrier in Phase Disposition (IPD) PWM Method

The multicarrier IPD method is similar to the multicarrier APOD method whereas in this method the carrier signals are in same phase and are arranged same as the above method and the functional method is same as explained in the above method is shown in **Figure 5**.

4.3. Multireference Pulse Width Modulation Method

In this method multi reference PWM technique is followed where it requires multiple reference signal and with

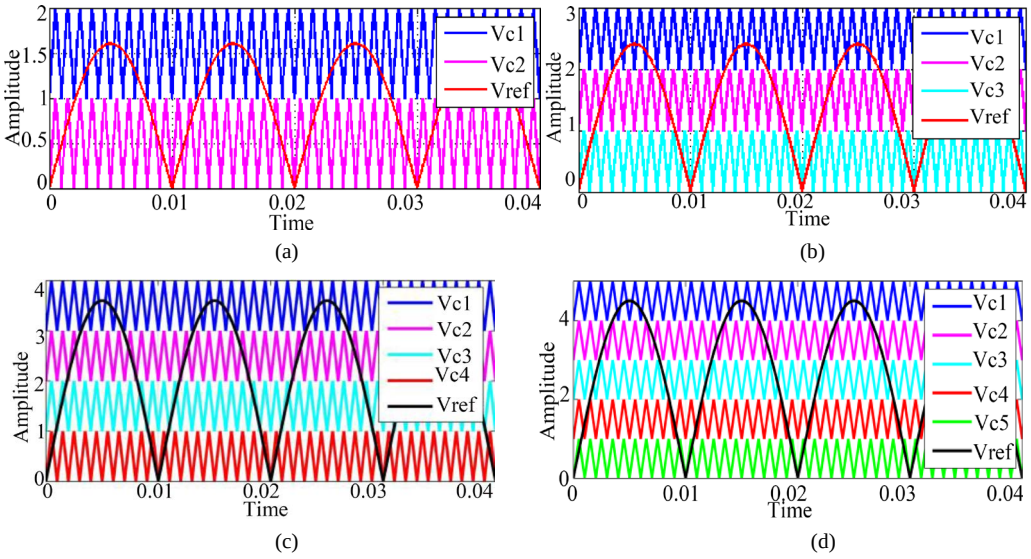


Figure 4. Carrier alignment of APOD PWM method for RSCMLI inverter of (a) Five Level; (b) Seven Level; (c) Nine Level; (d) Eleven Level.

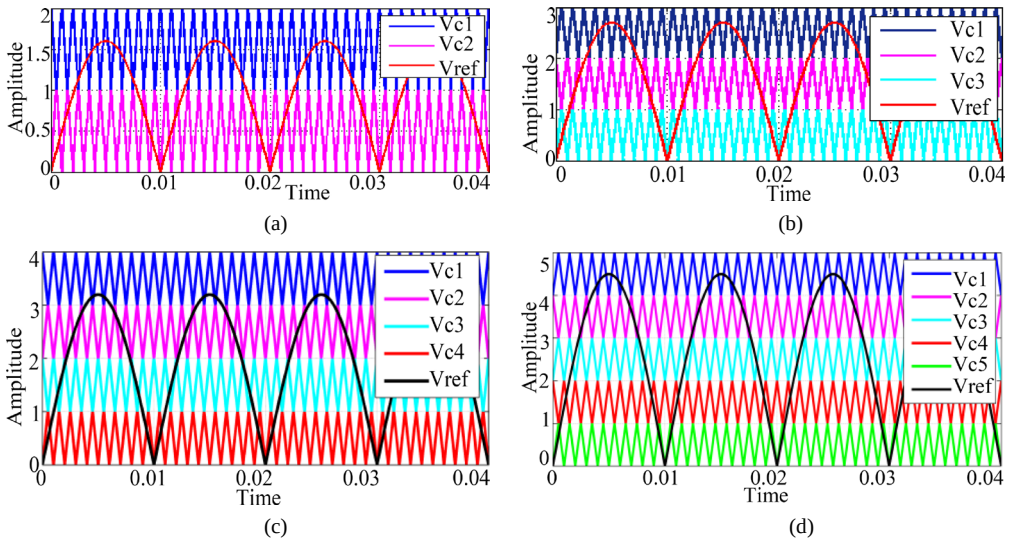


Figure 5. Carrier Alignment of IPD PWM method for RSCMLI inverter of (a) Five Level; (b) Seven Level; (c) Nine Level; (d) Eleven Level.

single carrier signal to generate gate pulse. This method [1] of PWM technique is already implemented for nine level inverter for this RSCMLI in [15] for DSTATCOM and the method is discussed in detail is followed in this paper. It has (N − 1)/2 reference signals which are of same frequency with equal amplitude and were in phase with an offset value equal to the magnitude of the carrier signal. The reference signals were compared with a carrier signal to generate gate pulses for the switches. For the eleven level inverter it has five reference (V_{ref1}, V_{ref2}, V_{ref3}, V_{ref4}, and V_{ref5}) signals and with a carrier signal ($V_{carrier}$). V_{ref1} is compared with $V_{carrier}$ if V_{ref1} exceeds the magnitude of carrier signal $V_{carrier}$ then V_{ref2} is compared with the carrier signal till it exceeds the peak magnitude of $V_{carrier}$ then V_{ref3} is compared with the carrier signal until it exceed the peak magnitude of the carrier signal then V_{ref4} is compared with the carrier signal till it has exceed the magnitude of the carrier signal $V_{carrier}$ then V_{ref5} is compared with the carrier signal until it reaches zero then V_{ref4} is compared with the carrier signal till it reaches zero then V_{ref3} is compared with $V_{carrier}$ until it has reached zero then V_{ref2} is compared with $V_{carrier}$ till it reaches zero then onwards V_{ref1} is compared with $V_{carrier}$ signal. This method is shown in **Figure 6**.

The switching sequences for five, seven, nine and eleven level of RSCMLI are given in **Tables 1-4**.

These techniques are implemented for five level, seven level, nine level and eleven level RSCMLI inverter and the harmonic analysis are carried out for these methods.

5. Simulation Results

5.1. Harmonic Analysis of the RSCMLI Inverter

The harmonic analysis of the reduced switch count MLI inverter is carried out with the PWM techniques of multicarrier APOD, IPD method and with multireference PWM technique for five level, seven level, nine level

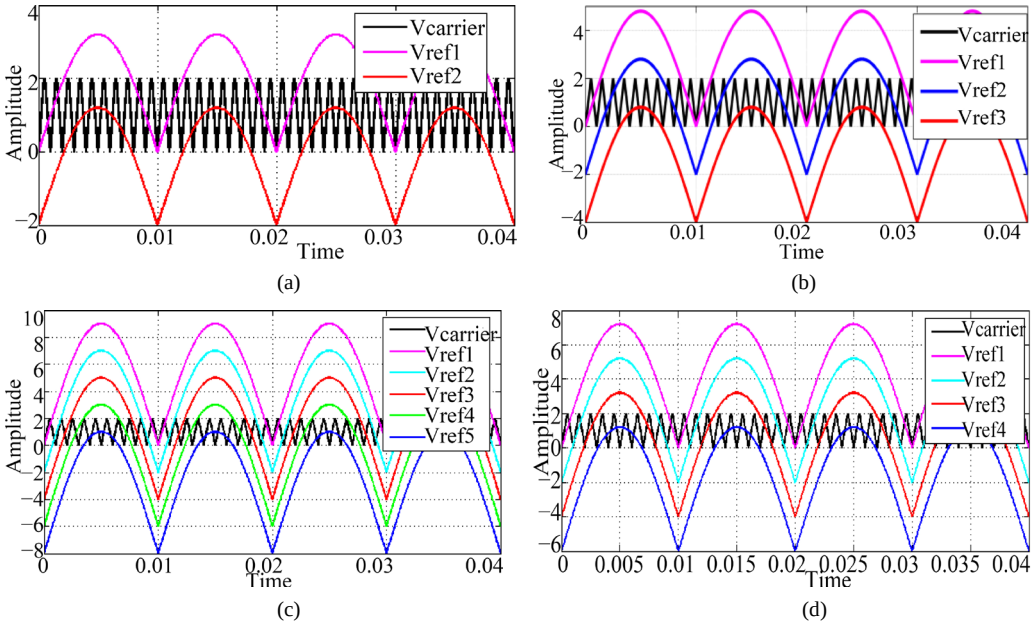


Figure 6. Multireference PWM method for RSCMLI inverter of (a) Five Level; (b) Seven Level; (c) Nine Level; (d) Eleven Level.

Table 1. Switching sequence for five level RSCMLI topology.

Output Voltage	S1	S2	S3	S4	S5
+Vdc/2	0	0	0	1	1
+2Vdc/2	1	0	0	1	0
0	1	1	0	0	0
−Vdc/2	0	1	0	0	1
−2Vdc/2	0	1	1	0	0

Table 2. Switching sequence for seven level RSCMLI topology.

Output Voltage	S1	S2	S3	S4	S5	S6
+Vdc/3	0	0	0	1	0	1
+2Vdc/3	0	0	0	1	1	0
+3Vdc/3	1	0	0	1	0	0
0	1	1	0	0	0	0
−Vdc/3	0	1	0	0	1	0
−2Vdc/3	0	1	0	0	0	1
−3Vdc/3	0	1	1	0	0	0

Table 3. Switching sequence for nine level RSCMLI topology.

Output Voltage	S1	S2	S3	S4	S5	S6	S7
+Vdc/4	0	0	0	1	0	0	1
+2Vdc/4	0	0	0	1	0	1	0
+3Vdc/4	0	0	0	1	1	0	0
+4Vdc/4	1	0	0	1	0	0	0
0	1	1	0	0	0	0	0
−Vdc/4	0	1	0	0	1	0	0
−2Vdc/4	0	1	0	0	0	1	0
−3Vdc/4	0	1	0	0	0	0	1
−4Vdc/4	0	1	1	0	0	0	0

Table 4. Switching sequence for eleven level RSCMLI topology.

Output Voltage	S1	S2	S3	S4	S5	S6	S7	S8
+Vdc/5	0	0	0	1	0	0	0	1
+2Vdc/5	0	0	0	1	0	0	1	0
+3Vdc/5	0	0	0	1	0	1	0	0
+4Vdc/5	0	0	0	1	1	0	0	0
+5Vdc/5	1	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0
−Vdc/5	0	1	0	0	1	0	0	0
−2Vdc/5	0	1	0	0	0	1	0	0
−3Vdc/5	0	1	0	0	0	0	1	0
−4Vdc/5	0	1	0	0	0	0	0	1
−5Vdc/5	0	1	1	0	0	0	0	0

and eleven level for the modulation index of 1, 0.9 and 0.8. The voltage waveform of these levels with the PWM techniques and the FFT analysis are shown in **Figures 7-10** and the results are also compared with the Cascaded H-bridge Multilevel inverter. The results are tabulated in **Table 5**.

The result shows that the harmonic level is less in RSCMLI method compared to Cascaded H Bridge MLI. The RSCMLI with APOD PWM method for nine level is applied for DSTATCOM.

5.2. DSTATCOM for Power Factor Improvement with RSCMLI

The nine level reduced switch count multilevel inverter is used for the application of DSTATCOM in the voltage source inverter (VSI) part for power factor improvement in a nonlinear load connected system and the simulation model of the test system is shown in **Figure 11(a)** and the data are given in **Appendix**. Three phase source system of 415 V, 50 Hz is connected to the nonlinear load of rectifier unit with RC load and with the balanced linear load through source impedance. The nonlinear load in the system causes distortion in the current waveform occurs due to the current drawn from the system and affects the power factor and harmonic level. To improve the power factor and the harmonic level, DSATCOM is connected to the system at PCC point through coupling transformer. The controller used for the DSTATCOM is based on dq frame based current controller and is shown in **Figure 11(b)**.

The analysis of the system without and with DSTATCOM for power factor improvement is carried out and the simulation results are shown in **Figures 12-16** and are tabulated in **Table 6**.

Figure 12 shows the waveform of source voltage and current when the system is connected to the nonlinear load. **Figure 13** shows the voltage and current waveform at load point when it connected to the nonlinear load. The waveform shows that with nonlinear load the current gets distorted and disturbance in the voltage waveform, this reduces the power factor of the system and increase in the harmonic level.

Figure 14 shows the waveform of source voltage and current when the system is connected to nonlinear load and with DSTATCOM, the result shows that the current waveform is improved without distortion. **Figure 15** shows the waveform of voltage and current at PCC point with DSTATCOM, result shows that the current waveform have improved to sinusoidal from distorted waveform and the harmonic level of it also improved as listed in **Table 6** and the voltage and current waveform at load point with DSTATCOM is shown in **Figure 16**.

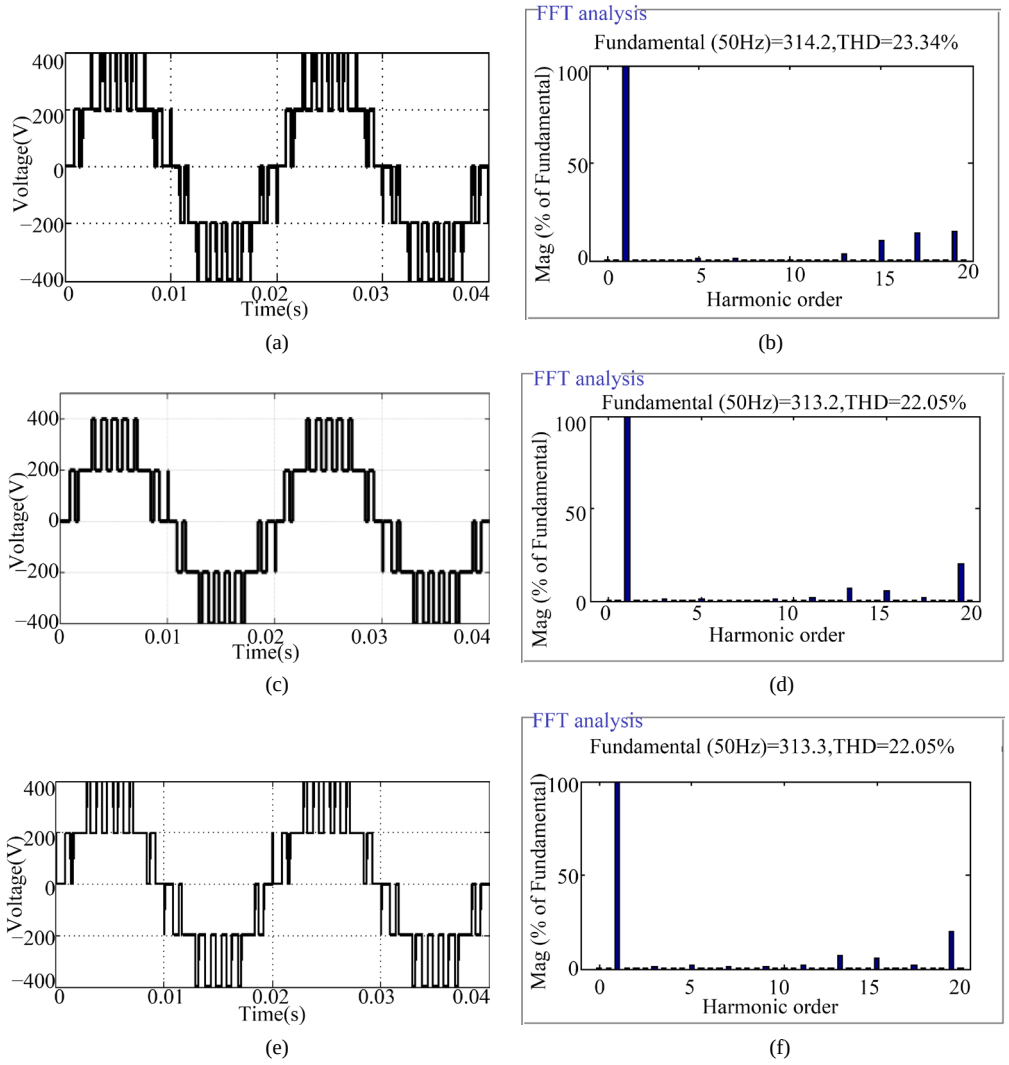
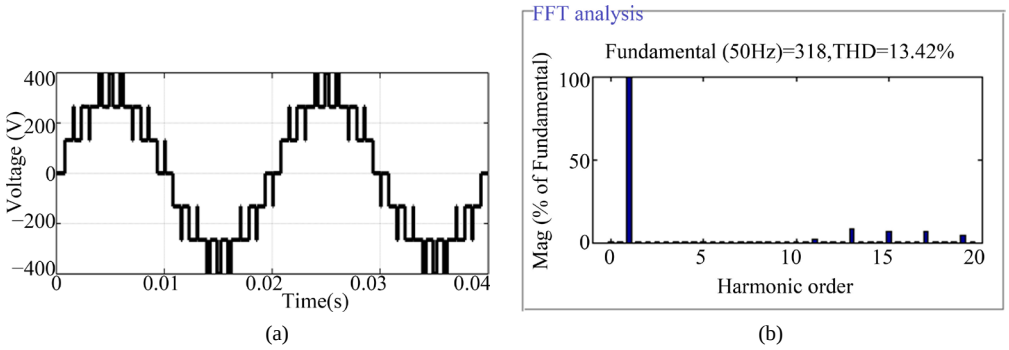


Figure 7. Voltage waveform for five level RSCMLI with (a) APOD PWM method, (c) IPD PWM method, (e) Multireference PWM method and its FFT analysis for harmonic level respectively in (b), (d), (e).



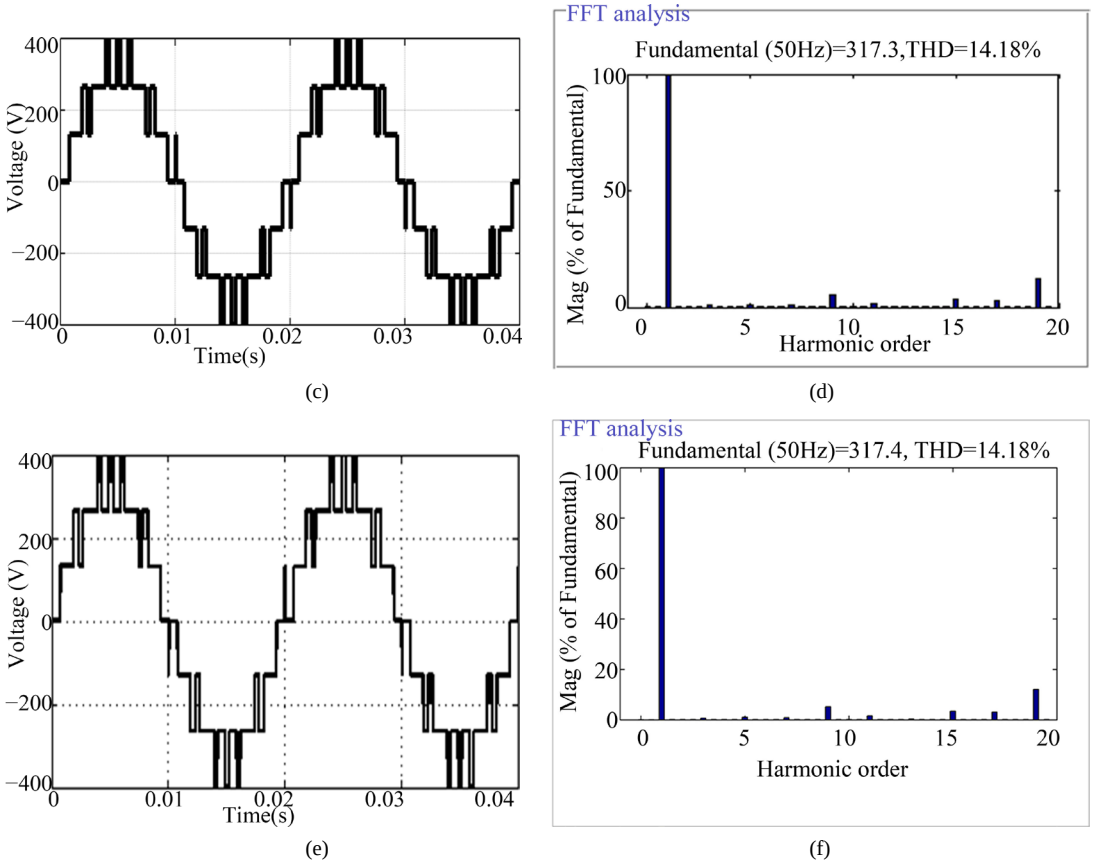
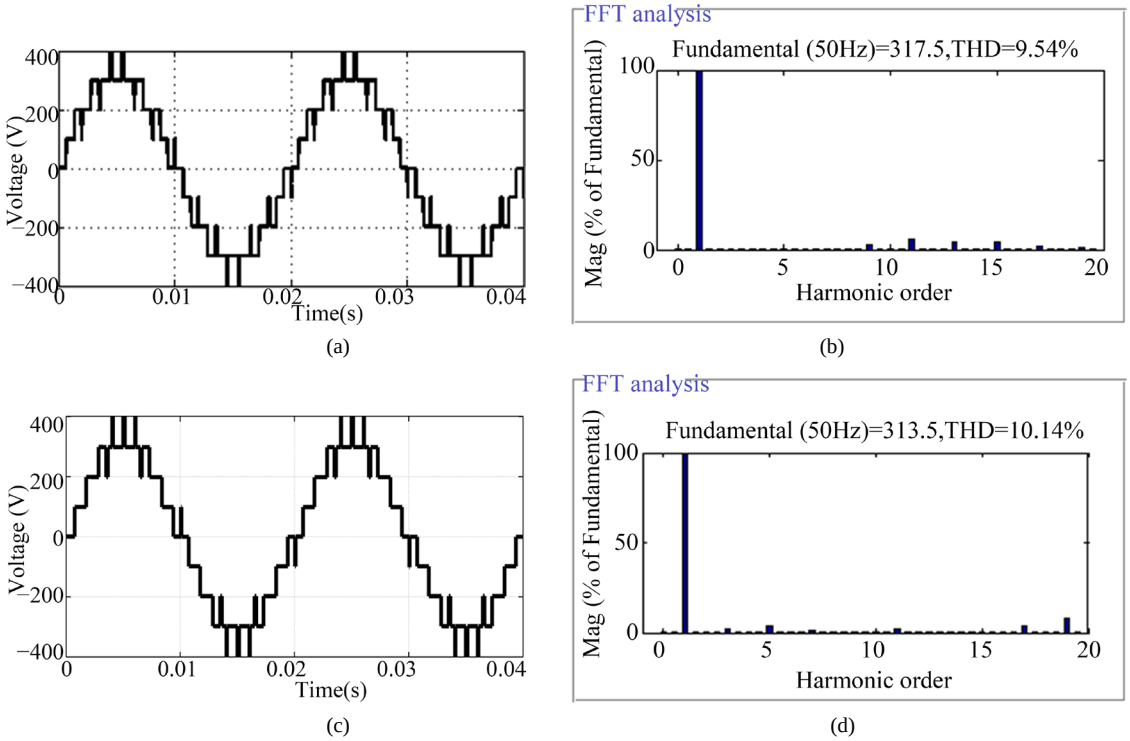


Figure 8. Voltage waveform for Seven Level RSCMLI with (a) APOD PWM method, (c) IPD PWM method, (e) Multireference PWM method and its FFT analysis for harmonic level respectively in (b), (d), (e).



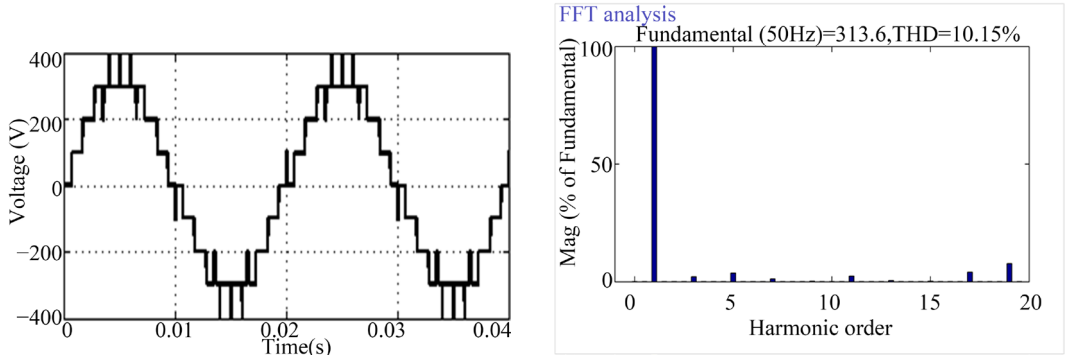


Figure 9. Voltage waveform for Nine Level RSCMLI with (a) APOD PWM method, (c) IPD PWM method, (e) New PWM method and its FFT analysis for harmonic level respectively in (b), (d), (e).

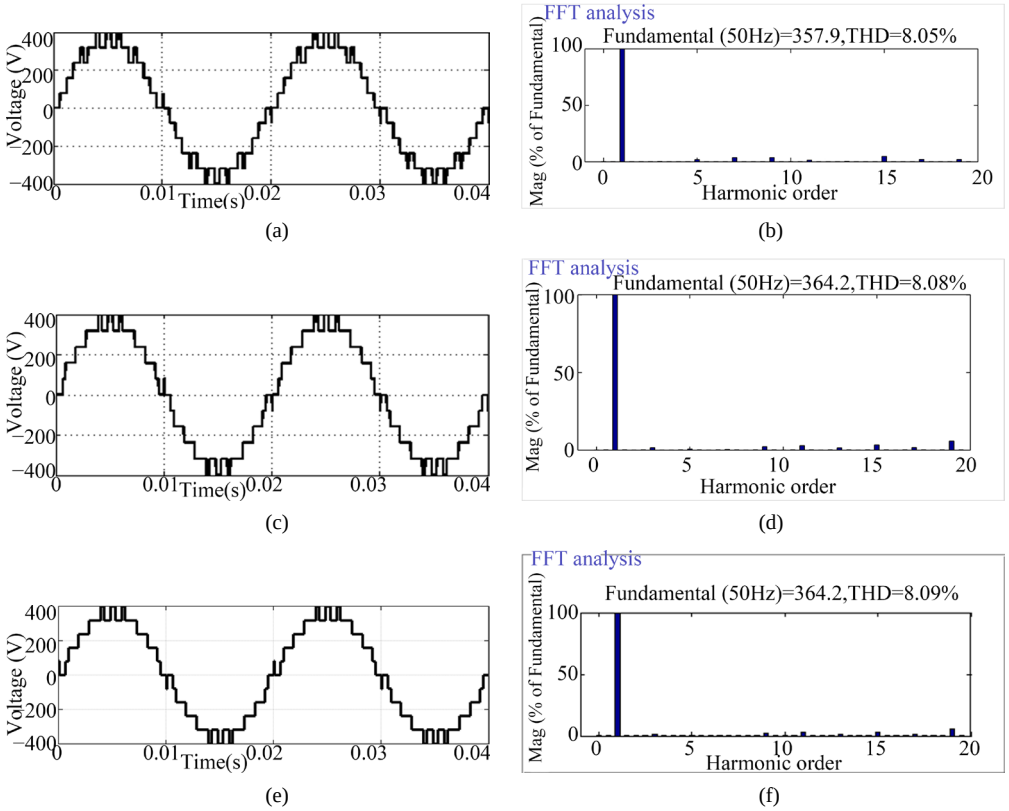


Figure 10. Voltage waveform for Eleven Level RSCMLI with (a) APOD PWM method, (c) IPD PWM method, (e) New PWM method and its FFT analysis for harmonic level respectively in (b), (d), (e).

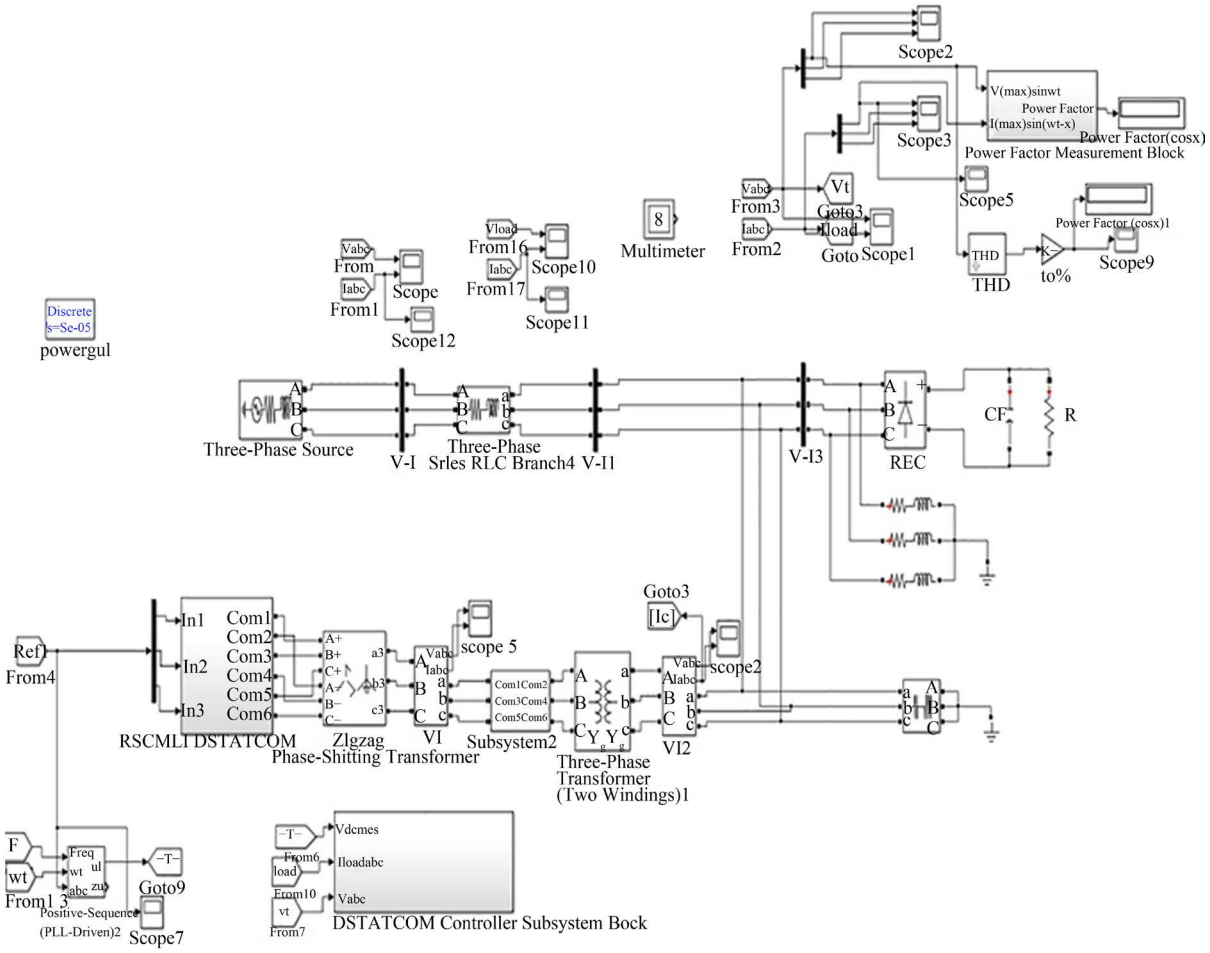
The harmonic level of the voltage and current of the system with nonlinear load when the system is connected without DSTATCOM and with DSTATCOM is tabulated in **Table 6**. DSTATCOM is connected to the system for the improvement of power factor and to minimize the harmonic level of the system.

6. Conclusion

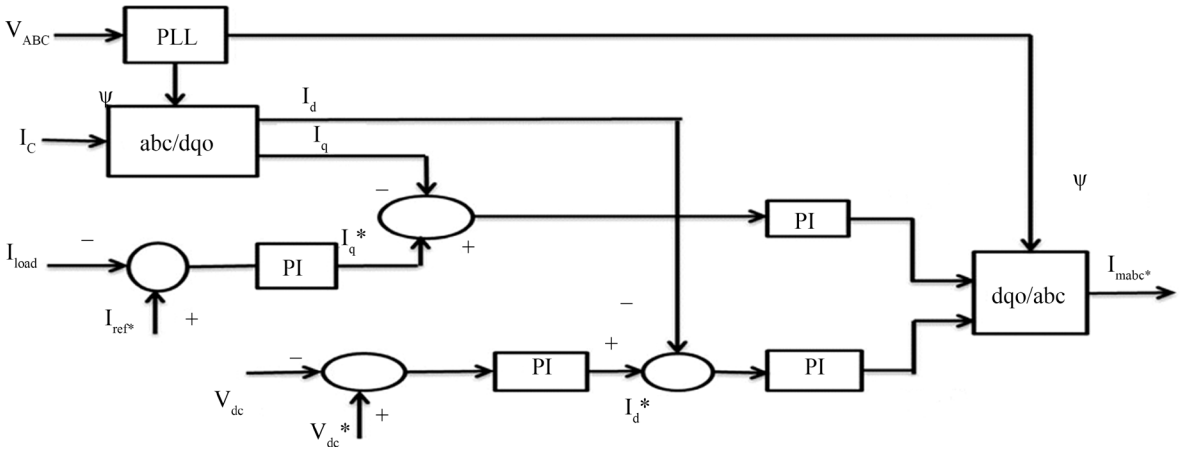
In this paper, the Reduced Switch Count Multilevel Inverter (RSCMLI) structure topology is analyzed with the Alternate Phase Opposition Disposition method (APOD), In Phase Disposition method (IPD), and with multi reference PWM method. The harmonic analysis for five level, seven level, nine level and eleven level of RSCMLI inverter is carried out with these PWM techniques for the modulation index of 1, 0.9 and 0.8.The re-

Table 5. Comparison of Harmonic Level between RSCMLI and CHBMLI for different PWM Technique with different Modulation Index.

Levels	Modulation Index	APOD PWM Method		IPD PWM Method		THD of RSCMLI with Multireference PWM Method (in %)
		THD of RSCMLI (in %)	THD of CHBML (in %)	THD of RSCMLI (in %)	THD of CHBMLI (in %)	
Five Level	1	14.86	16.02	14.41	19.20	14.43
	0.9	19.67	23.05	19.17	26.28	19.21
	0.8	23.34	26.01	22.05	31.26	22.11
Seven Level	1	10.27	11.05	10.66	12.87	10.66
	0.9	13.36	14.01	13.08	17.88	13.08
	0.8	13.42	18.77	14.18	18.25	14.18
Nine Level	1	8.37	9.31	10.61	9.81	10.61
	0.9	9.75	10.66	12.15	11.54	12.15
	0.8	9.54	9.71	10.14	10.50	10.15
Eleven Level	1	7.38	7.50	7.84	8.09	7.85
	0.9	8.05	8.10	8.08	10.44	8.09
	0.8	8.32	8.41	10.60	10.95	10.61



(a)



(b)

Figure 11. (a) Simulink model of the DSTATCOM system; (b) Block diagram of DSTATCOM controller.

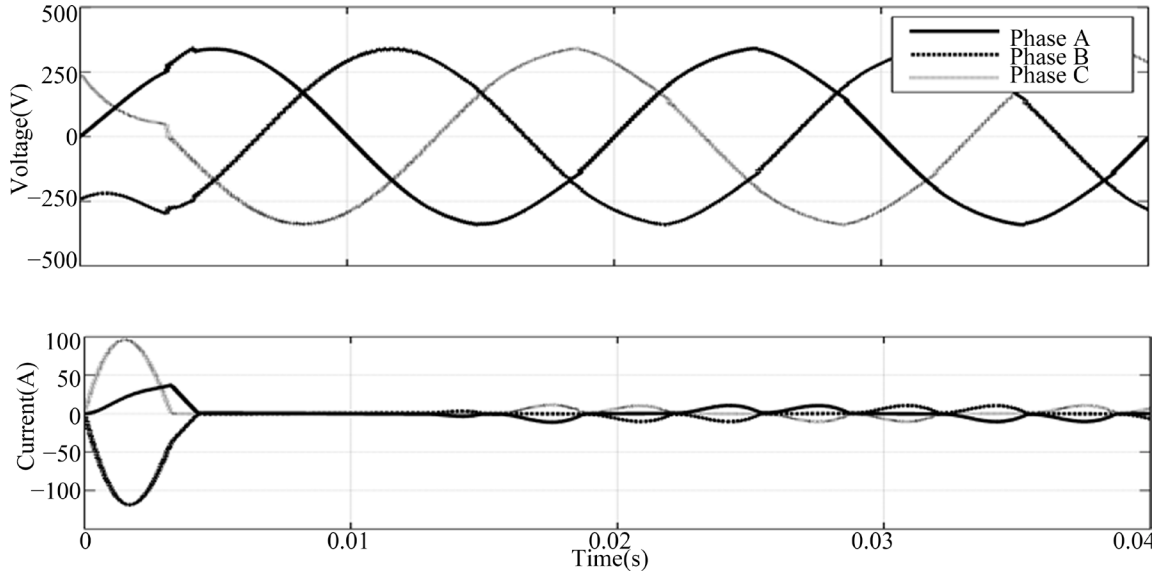


Figure 12. Voltage and current waveform of the system at source point with nonlinear load.

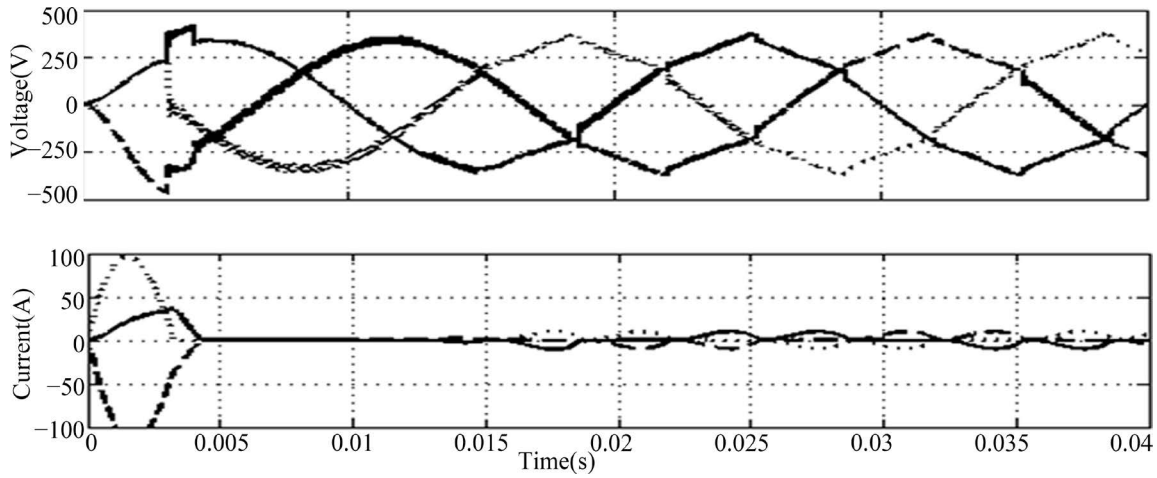


Figure 13. Voltage and current waveform of the system at load point with nonlinear load.

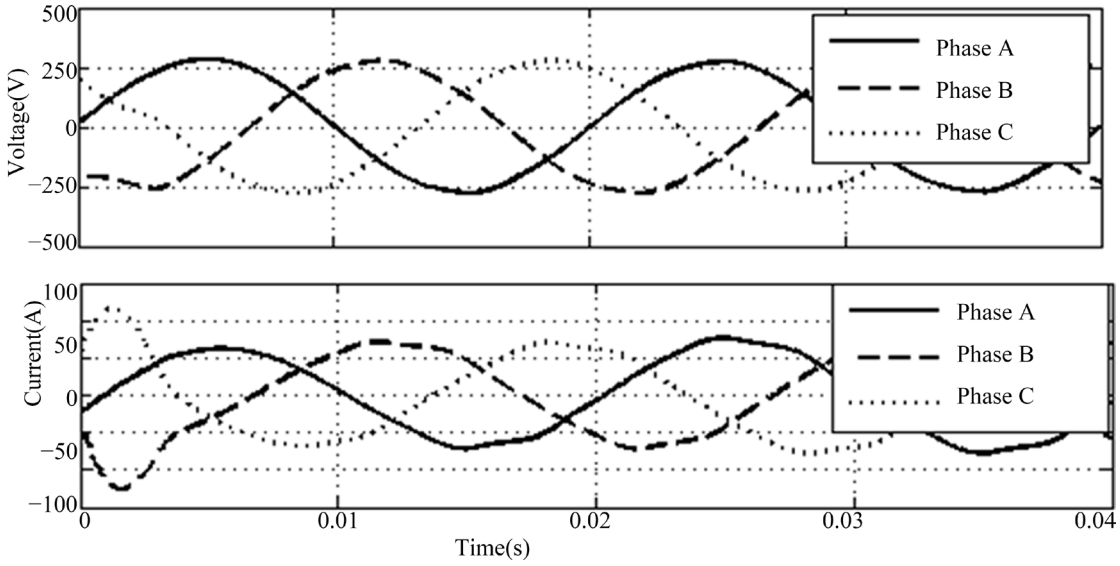


Figure 14. Voltage and current waveform of the system at source point with DSTATCOM.

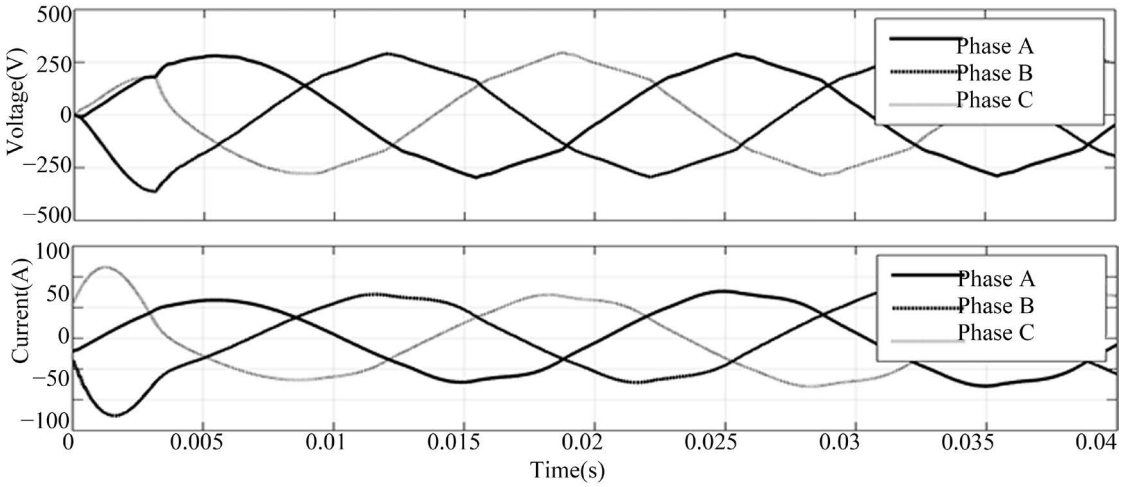


Figure 15. Voltage and current waveform of the system at PCC point with DSTATCOM.

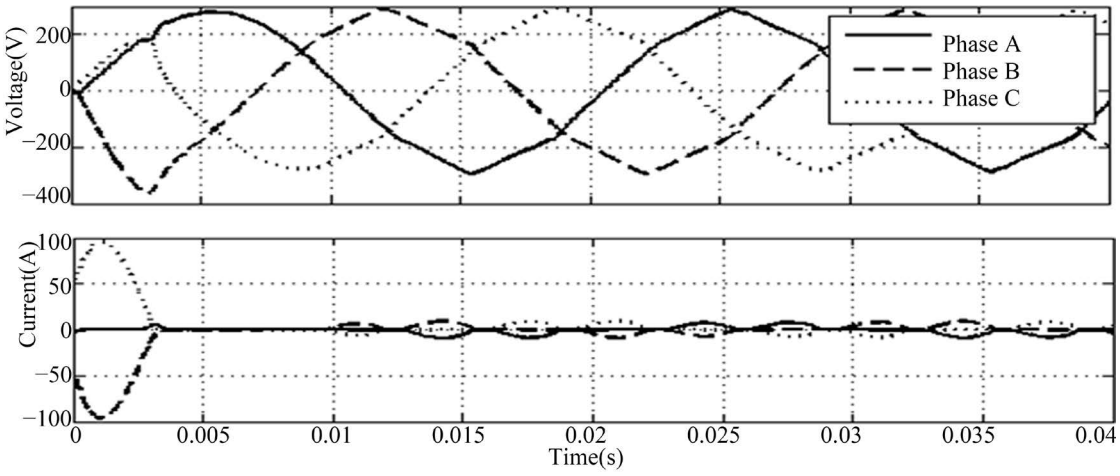


Figure 16. Voltage and current waveform of the system at load point with DSTATCOM.

Table 6. Comparison of harmonic level of the nonlinear load system without and with DSTATCOM.

Parameters	Without DSTATCOM	With DSTATCOM
THD of Voltage at source point	2.83%	1.25%
THD of current at source point	124.04%	4.53%
THD of Voltage at PCC point	8.20%	3.94%
THD of current at PCC point	124.40%	4.53%
THD of Voltage at load point	8.20%	3.94%
THD of current at load point	136.39%	91.61%
Power Factor	0.8339	0.9985

sults are tabulated in **Table 5** and are compared with the APOD and IPD method of CHBMLI topology, the result shows that the RSCMLI provides better harmonic level. Among the three PWM methods for RSCMLI, the APOD methodology provides reduced harmonic level. This RSCMLI nine level inverter with APOD PWM method is used for the application of DSATCOM to improve power factor and harmonic level when the three phase system is connected to the nonlinear load. The nonlinear load connected to the system distorts the current waveform due to the harmonic current drawn from it. This leads to poor power factor and increase in harmonic level. DSTATCOM connected in shunt with the utility system improves power factor and harmonic level. The harmonic level of the voltage and current waveform is tabulated in **Table 6**. With the DSTATCOM, the power factor is improved from 0.8339 to 0.9985. The harmonic level of voltage at PCC is reduced from 8.20% to 3.94% and for current waveform it will be of 4.53% with DSTATCOM.

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Appendix

Three phase source: 415 V, 50 Hz; Source impedance = 0.001 Ω, L = 2e − 3H; Nonlinear load: Rectifier unit with RC load R = 100 Ω, C = 370e − 6F.Vdc = 400 V

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