Circuits and Systems, 2016, 7, 1307-1323
Published Online June 2016 in SciRes. http://www.scirp.org/journal/cs
http://dx.doi.org/10.4236/cs.2016.78114

A New Fully Differential Adaptive CMOS Line Driver Using Fuzzy Controller Suitable for ADSL Modems

Ali Dadashi, Yngvar Berg, Omid Mirmotahari

Department of Informatics, University of Oslo, Oslo, Norway
Email: alidada@ifi.uio.no

Received 12 February 2016; accepted 10 March 2016; published 8 June 2016

Abstract

In this paper, a new principle for an adaptive line driver using Fuzzy logic is presented. This type of line driver can adapt its output impedance and gain, automatically to the applied load using a fuzzy logic controller (FLC). This results in automatically corrected output impedance for different cables with terminations. Also, the line driver output impedance and gain become insensitive to process and line variations. As an example, a line driver for ADSL application has been designed. The circuit operates from a 3.3 v in a 0.35 um standard CMOS technology. The power consumption of FLC is about 1 mW. The circuit dissipates 106 mW and exhibits a −62 dB THD for a 3.2-Vpp signal at 5 MHz across a 75 ohms Load. It has a relatively high −3 dB bandwidth (240 MHz) with good phase margin of about 67 degrees in a 10 pF load capacitor.

Keywords

Fuzzy Logic Controller (FLC), ADSL Modem, Adaptive Line Driver, Folded Cascode Power Supply Noise, Class A/B

1. Introduction

As the demand for communication systems increases, the possibility of transmission data over the old telephone lines also increases. DSL system is the most important method to communicate high rate information over the telephone lines. ADSL modems are designed to provide signal bit-rates up to 6.4 Mbps for home use. ADSL modems are asymmetric, in which receive and transmit signal BW are 138 KHz, and 1104 KHz, respectively. In ADSL Modems, as shown in **Figure 1**, High-speed, high linear line drivers are highly needed. In most ADSL modems, line drivers are fabricated in Bipolar or BICMOS technology when high current driving capability is

How to cite this paper: Dadashi, A., Berg, Y. and Mirmotahari, O. (2016) A New Fully Differential Adaptive CMOS Line Driver Using Fuzzy Controller Suitable for ADSL Modems. *Circuits and Systems*, **7**, 1307-1323.
http://dx.doi.org/10.4236/cs.2016.78114

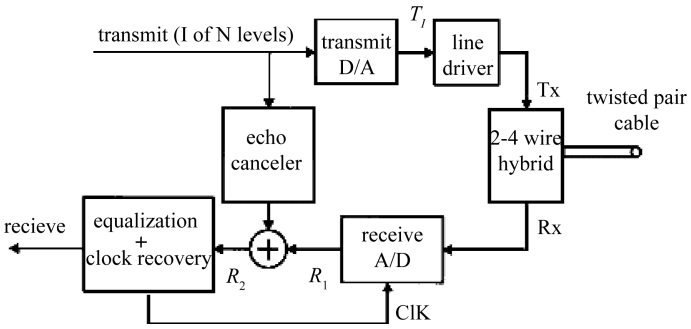


Figure 1. This main blocks of a transceiver.

important. But a great trend exists in designing CMOS line drivers to achieve a full CMOS AFE (analog front end) on a chip. Line drivers (LD) are op-amps, but with higher current-driving capability of very low resistive loads. In LDs, output stage is the most important component compared to the other parts of the LD. In most LDs, class-AB output stages preferred to the other output stage classes. The load which is nominally between 50 and 100 varies upon the cable length, temperature and other external effects, and this causes the reflections in the line. To minimize reflections, the source and load impedances of the transmission line have to be equal to the characteristic impedance of the line. In traditional architectures, there is a 6-dB signal loss incurred in the external resistors that implement cable termination which adds to the inefficiency of the driver [1]. An approach that provides integrated termination with no signal loss in the termination is also a desirable feature for LDs. In this paper, a novel method for an adaptive LD based on Fuzzy logic controller (FLC) with no signal loss in termination is introduced. An adaptive tuning scheme for output impedance matching using peak detection is used to provide uniform performance across line impedance variations. The use of fuzzy systems is widespread, mainly in the control field. Furthermore, in many applications the knowledge describing the expected behavior of the system is contained on data clusters. Due to this, the designer has to elaborate the IF-THEN rules according to such data; if the data clusters are too large, it could imply a tremendous effort. Neural networks can learn from data clusters, so it results natural thinking in a methodology which gathers the characteristics of both systems, combining explicit knowledge representation of fuzzy logic with the learning capability of neural networks. In this way, the called neuro-fuzzy systems are obtained. Among the various inference methods reported in the literature, the singleton or zero-order Takagi-Sugeno-Kang's (TSK) method is very adequate for hardware implementations. Functionally, the ANFIS architecture is equivalent to a TSK zero order and/or first order fuzzy system [2]. In [3], ANFIS architecture is discussed and optimized using a new algorithm. This algorithm is suited to use in CMOS circuits. In this paper, a two input, one output current mode FLC based on [4] is designed. In this structure the output impedance and gain of the LD can be controlled by using a Fuzzy controller.

This paper is organized as follows: in Section 2 the blocks of the LD are explained and the circuit specifications, such as the differential gain and frequency response are calculated. Also a circuit to compensate temperature, process variations and supply noise is proposed in this Section. In Section 3, the FLC used in this structure is explained. Simulation results are reported in Section 4. Finally, Section 5 concludes the paper.

2. LD Design

Figure 2 shows the simplified schematic of the closed loop part of the LD (without tuning circuit). By assuming that the amplifier's gain is high, the overall gain depends on resistance feedback network and it is obviously equal to:

$$\frac{Vo_{diff}}{Vi_{diff}} = -\frac{R_{f1}}{R_{f2}} \tag{1}$$

Ratio of two resistors, and hence closed-loop gain, is independent of temperature and process variations to a great extent. In this design, the closed-loop gain was designed to be one. **Figure 3** shows the simplified schematic of the LD without tuning circuit, common- mode feedback and bias circuits. Proposed LD consists of a gain stage and output stage. First stage is a preamplifier that is a folded cascode amplifier and second stage is a widely used class A/B output stage. The dc-gain of the designed LD is equal to:

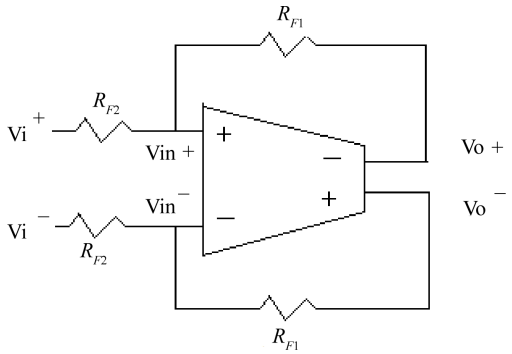


Figure 2. Simplified schematic of the closed loop part of the LD, that is not tunable.

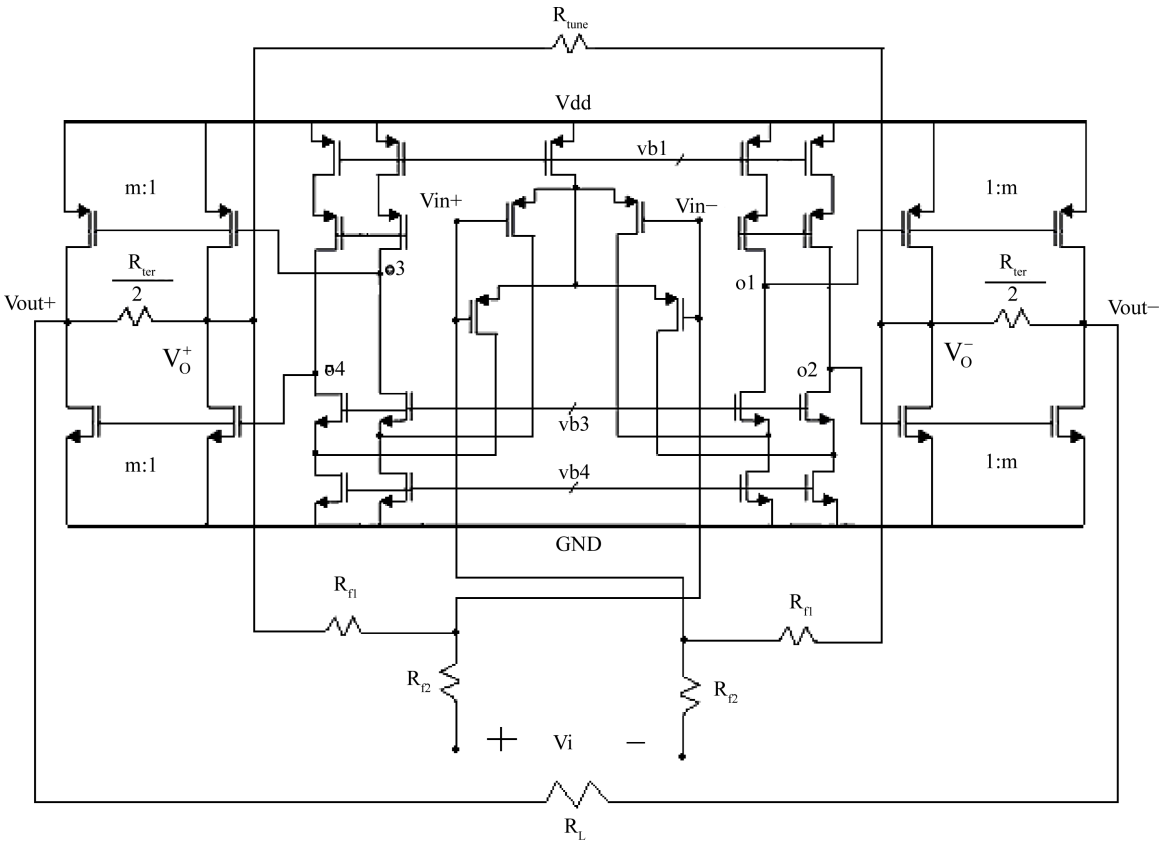


Figure 3. Complete schematic of the LD (without tuning circuit).

$$A_{vf0} = A_{v1} \times A_{v2} \tag{2}$$

and A_{v1}, A_{v2} are the dc-gain of the first stage and output stage, respectively. The Polysilicon resistance is used to implement circuit resistors because it is more linear than others (p-well or n-well resistances). Because of using fully differential architecture, common-mode disturbances, such as substrate or power supply noise are cancelled to a great extent. In addition, even order harmonics are also eliminated. In this work, two separate common-mode feedback circuits are used in the two stages due to fast transient, instead of using an overall common-mode feedback which is usually slow. This helps to achieve a much reduced distortion [5].

2.1. First Stage of the LD

Figure 4 shows the first stage of the LD. Devices M1-M21 forms the two well known folded cascode op-amps

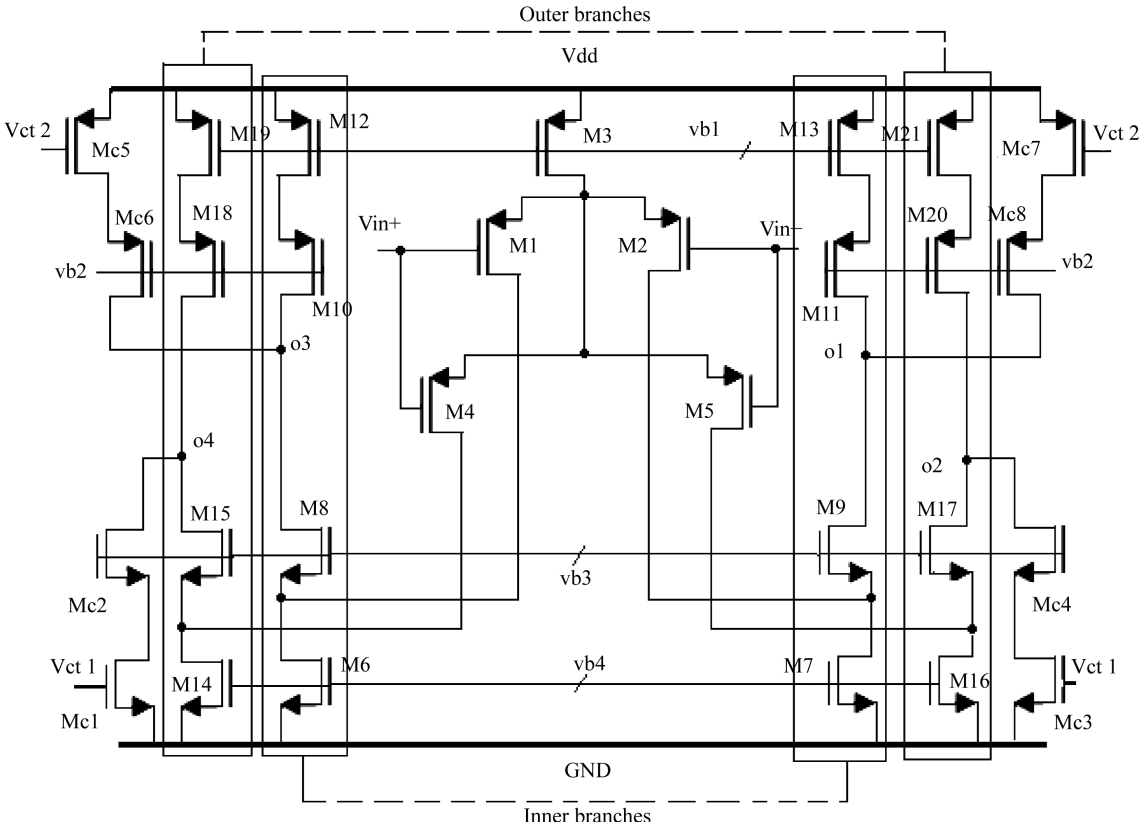


Figure 4. First stage of the LD.

as preamplifiers. The dc-gain of this amplifier is approximately:

$$A_{v1} = g_{mM1} \times R_{out1} \tag{3}$$

$$R_{\text{out1}} \approx \left[g_{mM10} \times r_{oM10} \times r_{oM12}\right] \left\| \left[g_{mM8} \times r_{oM8} \times \left(r_{oM6} \left\| r_{oM1}\right.\right)\right] \right\| \left[g_{mMc6} \times r_{oMc6} \times r_{oMc5}\right] \tag{4}$$

To save power in [6], the structure shown in **Figure 5** is used. Two resistors (R1, R2) are used to provide a dc-shift between the gate voltages of NMOS and PMOS devices of output stage. This structure results in a significant reduction in the bias current of the output stage devices. It is clear that in the LDs the output stages consumes the dominant portion of the power. So the static power of the LD reduces because of a significant reduction in bias currents of output stage devices. But these resistors limit the bandwidth of the LD. Also using capacitors parallel with the resistors in [6] (**Figure 5**) increases the settling time of the LD by introducing a pole-zero doublet to frequency response of the LD. In the proposed LD, two op- amps of the first stage are in different output common-mode voltage levels, to provide a dc-shift between the gate voltages of NMOS and PMOS output stage devices. This dc-shift reduces the static power consumption of the circuit by reducing the bias currents of the output stage devices as well as resistors in [6]. Therefore the dc-shift (Vref2-Vref1) for gate voltages of output devices is provided and power consumption is reduced without any reduction in the bandwidth of LD. **Figure 6** shows the common-mode feedback circuits of the op-amps of first stage of the LD. For proper operation, the preamplifier with higher common-mode voltage level (O1, O3), has a NMOS type common-mode feedback circuit (**Figure 6(a)**). Circuit for generating Vref1 and Vref2 is shown in **Figure 10**. This circuit will be investigated in detail in the end of this section. It can compensate the process and temperature variations for the LD circuit as well. To keep the output common-mode voltage of the outer branches of the first stage in Vref1, Vct1 is fed to gates of Mc1 and Mc3. The same process is done for inner branches, which means that, the control signal Vct2 is fed to the gate of Mc2 and Mc4. This type of common-mode feedback circuit is investigated in detail, in [6] and [7]. Except that with using cascode branches (e.g. Mc1, Mc2), the output currents of common-mode feedback circuits are applied directly to the output nodes of first stage, instead of cas-

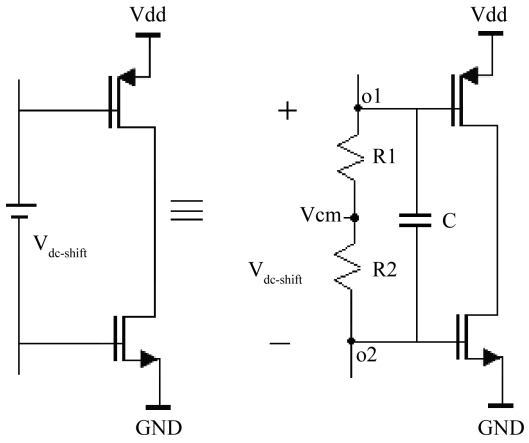


Figure 5. Dc-shift generator in [6].

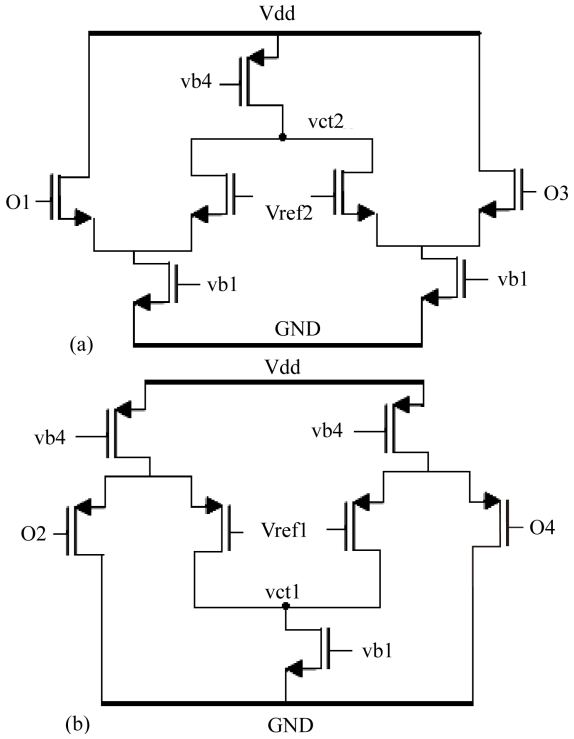


Figure 6. Common-mode feedback circuit of the first stage (a) Common-mode feedback circuit for branch with higher common-mode voltage level. (b) Common-mode feedback circuit for branch with lower common-mode voltage level.

code nodes in the conventional circuits (e.g. [6]). So the capacitance of cascode nodes is reduced and they will be faster nodes.

2.2. Second Stage of the LD

Figure 7 shows the complete schematic of the output stage of the LD without common-mode feedback circuits. As mentioned before, the second stage of the LD is a widely used class A/B power amplifier output stage, which delivers load current with some voltage gain.

Devices Mo1-Mo8 form the well known class A/B output stages in the differential mode. Notice that devices Mo1-Mo4 are out of the resistive feedback loop (**Figure 2**). Indeed the devices Mo1-Mo4 are used to tune output impedance of the line diver and force it to be equal with RL. By tuning the output impedance of the LD the cable impedance variations can be compensated and the reflections will be removed from the line. Mr1-Mr4 de-

vices are in the triode region, and form the tunable resistors. The gate voltage of these devices will be tuned with a FLC to correct the output impedance and gain of the LD. Impedance matching is done using a topology wherein, when the output voltage(Vout) is equal to the input, the output resistance is matched to the line [1] [8]. This scheme has the advantage that it can adjust to external line as well as internal process variations. The dc-gain of the output stage can be calculated as:

$$A_{v2} = \left(g_{mMo6} + g_{mMo8}\right) \times R_{\text{tune}} \tag{5}$$

From **Figure 7** and **Figure 8** the output impedance of the LD is achievable. To calculate the output impedance of the LD, test voltage (Vx) is applied to the output node (Vout) and the current produced is calculated. With writing a KCL in the output node (Equation (6)), and calculating Ix (current of Vx), the output impedance

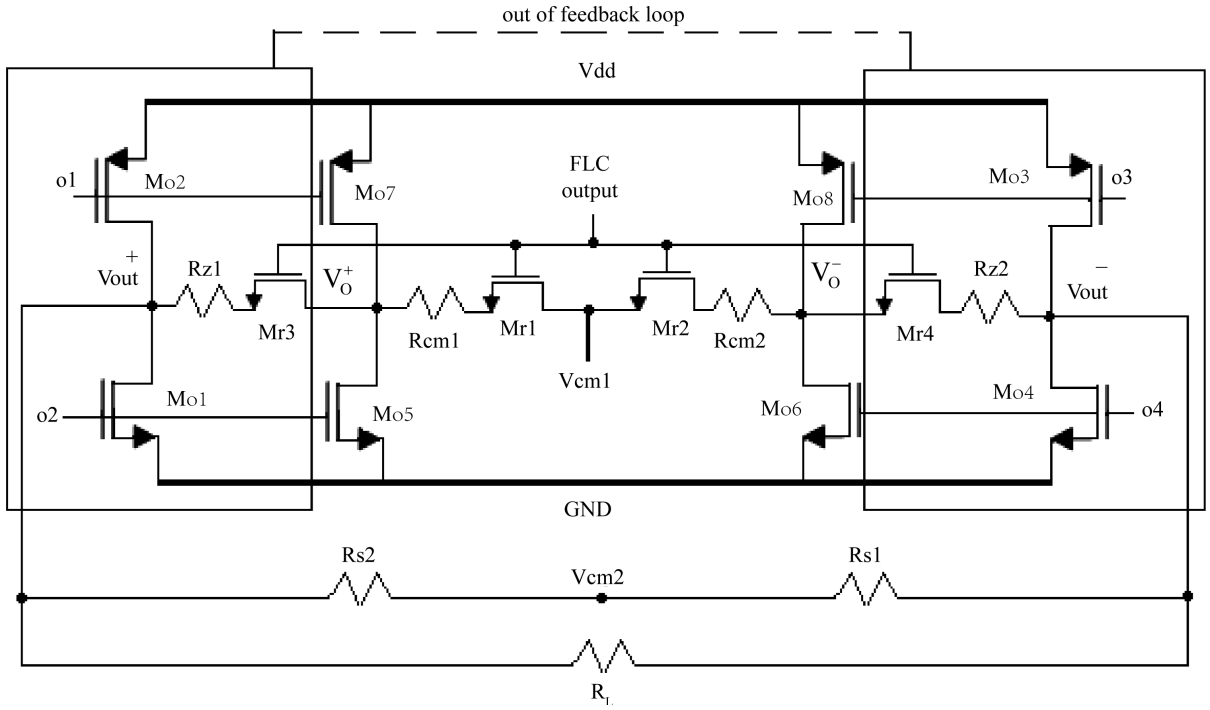


Figure 7. The tunable output stage of the LD.

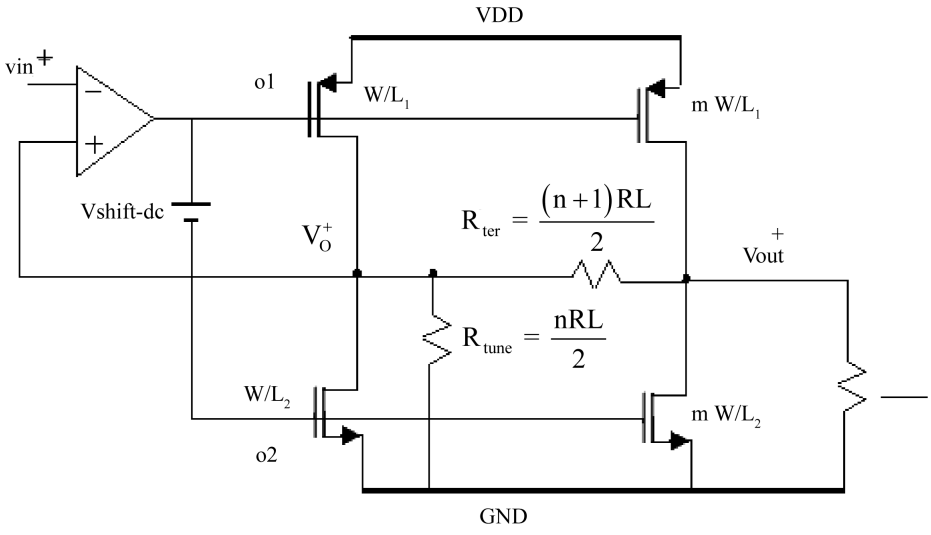


Figure 8. Simplified schematic of the LD.

is equal to Equation (7). (Notice that to calculate the output impedance, the Vo node is virtual ground because of the external resistive feedback network effect).

$$\left(\frac{Vx}{R_{ter}}\cdot m\right)+\frac{Vx}{R_{ter}}=Ix\Rightarrow R_{\text{out}}=\frac{Vx}{Ix}=\frac{R_{ter}}{(m+1)} \tag{6}$$

$$R_{\text{out}}=\frac{R_{ter}}{(m+1)}=\frac{\left(R_{z1}+R_{z2}+R_{M_{r3}}+R_{M_{r4}}\right)}{(m+1)} \tag{7}$$

$$R_{ter}=\left(R_{z1}+R_{z2}+R_{M_{r3}}+R_{M_{r4}}\right)=(n+1)\cdot R_L \tag{8}$$

Parameter *m*, is the size ratio of devices $Mo_{1,4}$ to $Mo_{5,6}$ and devices $Mo_{2,3}$ to $Mo_{7,8}$. Indeed this parameter (*m*) is the current mirroring ratio of the output stage devices. There is a trade off in the designing the parameter m. Larger m causes the larger parasitic capacitor in the output nodes of the first stage (o1, o2, 03, o4), and reduces the speed of the feedback loop and linearity in the higher frequencies. In the opposite side, larger m reduces the power consumption of the first stage by reducing the bias currents of the feedback loop devices. Considering this trade off, the optimum size can be found which gives good open-loop and closed-loop linearity and reasonable power consumption, by trial and error approach and considering the simulation results. According to this method, m is designed to be 30. The sizes of output stage devices are shown in **Table 1**. To calculate the voltage gain from V_o^+ to V_{out}^+ in **Figure 8** we can write:

$$\frac{Vo}{R_{\text{tune}}}\cdot m\cdot R_L=V_{\text{out}} \tag{9}$$

$$R_{\text{tune}}=\left(R_{cm1}+R_{cm2}+R_{Mr1}+R_{Mr2}\right)=n\cdot R_L \tag{10}$$

$$A_v=\frac{V_{\text{out}}}{V_o}=\frac{m\cdot R_L}{R_{\text{tune}}}=\frac{m\cdot R_L}{\left(R_{cm1}+R_{cm2}+R_{M_{r1}}+R_{M_{r2}}\right)} \tag{11}$$

and

$$R_{M_{r1,r4}}=\frac{L_{Mr1,Mr4}}{C_{ox}\mu W_{Mr1,Mr4}\left(Vgs_{Mr1,Mr4}-Vt_{Mr1,Mr4}\right)} \tag{12}$$

and $V_{gsMr1,Mr4}=\left(Vo_{FLC}-V_{cm1,2}\right)$
where V_{oFLC} is the output voltage of the FLC. And $V_{cm1,2}$ is the common-mode voltage of the output nodes which is equal to 1.65 volt. From Equations ((7)-(9), (11))

$$A_v=\frac{m\cdot R_L}{n\cdot R_L}=\frac{m}{n} \tag{13}$$

$$R_{\text{out}}=\frac{(n+1)R_L}{(m+1)} \tag{14}$$

And if the parameters *n* and *m* become equal (*n* = *m*), then: $A_v = 1$ and $R_{out}=R_L$. This condition happens by tuning Mr1-Mr4 devices with a FLC. In this case the termination (impedance matching) is done and reflections are eliminated. But if the impedance of the cable varies, the reflections appear in the line again and the performance of the driver will be degraded. The nominal value of RL is 75 Ω. To minimize reflections, the output impedance of the driver must be controlled and this can be performed by tuning of R_{ter} and R_{tune} with a FLC. It

Table 1. Size of transistors used in the output stage.

Transistor	*W* µm/*L* µm	Transistor	*W* µm/*L* µm
MO1	1200/0.35	MO5	40/0.35
MO2	3600/0.35	MO6	40/0.35
MO3	3600/0.35	MO7	120/0.35
MO4	1200/0.35	MO8	120/0.35

is clear that in this structure load variation directly changes the peak voltage of the output node (V_{out}^{+}). Hence for detecting load variations, the peak voltages of the input and output (V_{out}^{+}) nodes of the LD should be compared. Indeed the peak voltage of V_o^{+} is compared with peak voltage of V_{out}^{+}. It is clear that the common-mode voltage of the input voltage is not a constant value, so V_i^{+} and V_{out}^{+} do not have the same common-mode voltages and comparison of the positive peak voltages of these nodes is not reasonable. First input of the FLC is the difference of positive peak voltages of V_o^{+} and V_{out}^{+} nodes (e).

$$e = V_{\text{out}P-P}^{+} - V_{oP-P}^{+} \tag{15}$$

Another input of FLC, is the variation of the e (Δe). The voltage peak detector circuit is shown in **Figure 11**. Devices Mr1- Mr2 and Rcm1-Rcm2 have another role. They have been used in the output stage common-mode feedback loop. They provide the average voltage of the output nodes. Tuning these devices has a negligible effect on the performance of the output stage common-mode feedback circuit.

2.3. Frequency Response

The proposed LD has many poles and zeros, but two first poles or zeros are important in the frequency response of the op-amp. **Figure 9** is used for calculating frequency response of the LD. From **Figure 9**, the transfer function of closed loop part of the LD (A_{v1}) is:

$$A_{v1}(s) = \frac{V_o}{V_{\text{in}}}(s) = \frac{A_{vf0}}{\left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_2}\right)} \tag{16}$$

and A_{vf0} is dc-gain of the LD and is equal to:

$$A_{v_{f0}} = A_{v1} \times A_{v2} \tag{17}$$

By using miller effect [7] P_1, the pole which occurs in the output node of first stage is :

$$P_1 = -\frac{1}{R_{\text{out1}} \times C_{o1}} \tag{18}$$

$$C_{o1} \approx C_1 + A_{v2} \cdot C_{gdMo2} + A_{v2} \cdot C_{gdMo7} \tag{19}$$

$$C_1 = C_{dMc6} + C_{dM8} + C_{dM10} \tag{20}$$

$$R_{\text{out1}} \approx \left[g_{mM10} \times r_{oM10} \times r_{oM12}\right] \left\| \left[g_{mM8} \times r_{oM8} \times \left(r_{oM6} \left\| r_{oM1}\right.\right)\right] \right\| \left[g_{mMc6} \times r_{oM6} \times r_{oM5}\right] \tag{21}$$

and by using miller effect [7], P_2, the pole which occurs in the output node (V0+) is:

$$P_2 \approx -\frac{1}{\left(\left(\frac{c_1 + c_{gdMo7}}{c_{gdMo7} \cdot g_{mMo7}}\right) \| R_2\right) \times \left(\left(\frac{c_{gdMo7} \cdot c_1}{c_{gdMo7} + c_1}\right) + c_2\right)} \tag{22}$$

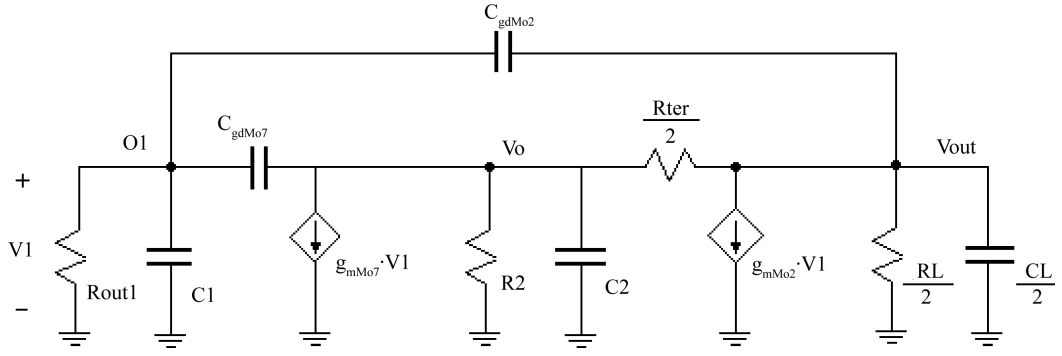


Figure 9. Used model in the calculating frequency response of the LD.

$$R_2 = \left(\frac{R_{\text{tune}}}{2}\right) \| r_{oMO5} \| r_{oMO7} \tag{23}$$

$$C_2 = C_{dM5} + C_{dM7} \tag{24}$$

Also from **Figure 9**, the total transfer function of the LD is:

$$A_v(s) = \frac{V_{\text{out}}}{V_{\text{in}}}(s) = \frac{A_{vf0}}{\left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_2}\right)} \tag{24}$$

where P_1 is equal to Equation (18) and by using miller effect, P_2 is:

$$P_2 \approx -\frac{1}{\left(\left(\frac{c_1 + c_{gdMo2}}{c_{gdMo2} \cdot g_{mMo2}}\right) \| R_{\text{out}}\right) \times \left(\left(\frac{c_{gdMo2} \cdot c_1}{c_{gdMo2} + c_1}\right) + c_{\text{out}}\right)} \tag{25}$$

$$C_{\text{out}} = \left(\frac{C_L}{2}\right) + C_{dMo6} + C_{dMo8} \tag{26}$$

$$R_{\text{out}} = \left(\frac{R_L}{2}\right) \| r_{oMO1} \| r_{oMO2} \tag{27}$$

In [6], load capacitor (C_L) is directly connected to the output node of the LD, and reduces the second pole of the LD which is occurred in the output node. Therefore the phase margin of the LD is also reduced by the load capacitor and also compensating of the LD, causes a reduction in the UGB and speed of the LD. But in the proposed structure opposite to [6], the load capacitor is out of the feedback loop and is not connected directly to the output node (V_o) of the feedback loop and does not reduce the phase margin of the LD. Therefore a fast feedback loop and so higher linearity in the higher frequencies can be achieved, in the same power consumption. It is considerable that the calculated frequency response in this section is correct only for a fixed load (impedance of the cable). It should be noted that a change in the load of the driver will result in a change in the frequency response of the driver.

2.4. Temperature and Process Variations and Power Supply Noise

Circuit for generating Vref1 and Vref2 (reference voltages of the first stage's common-mode feedback circuits) is shown in **Figure 10**. This circuit can compensate the process and temperature variation effects for output stage devices as well as the bias circuit in [6], but in this work, unlike in [6], there is not any resistor in the differential signal path (**Figure 10**). In the case of temperature variations the most sensitive parts of the LD are the large output stage devices. As the temperature increases the threshold voltage of these devices decreases. This variation causes to increase the bias current of the output stage devices and forces extra power consumption to the circuit. Furthermore temperature variations, force an extra distortion to the circuit. To reduce the effect of temperature variation in the bias current of the output devices, a technique is used in the circuit shown in **Figure 10**. As mentioned before the temperature increase, increases the bias current of the output stage devices, so the main idea is to prevent the bias current increase in these devices. By decreasing the gate-source voltages of these devices with temperature increase, the overdrive voltage of these devices will remain fixed to a great extent. As temperature increases, the bias current of M1 and M2 devices increase in the circuit of **Figure 10** as well as the current of output devices. Hence the voltage of V1 decreases in order to keep the current of M1 and M2 transistors constant. By decreasing the voltage of V1, the voltage of V2 decreases, too and so the current of reference resistor (R_{ref}) increases. This bias current increase happens in the M3-M9 devices and causes increase of the voltage drops on R1 and R2 resistors in the circuit of **Figure 10**. Hence the voltage difference between Vref1 and Vref2 (Vref1-Vref2) increases. As mentioned in sect.2.1, difference of the common mode voltages of the op-amps of the first stage increases. This causes a significant decrease in the bias current of the output stage devices by decreasing the gate-source voltages of these devices. By using this technique the effect of temperature increase in the increase of the bias current of the output devices is compensated and their bias currents remain

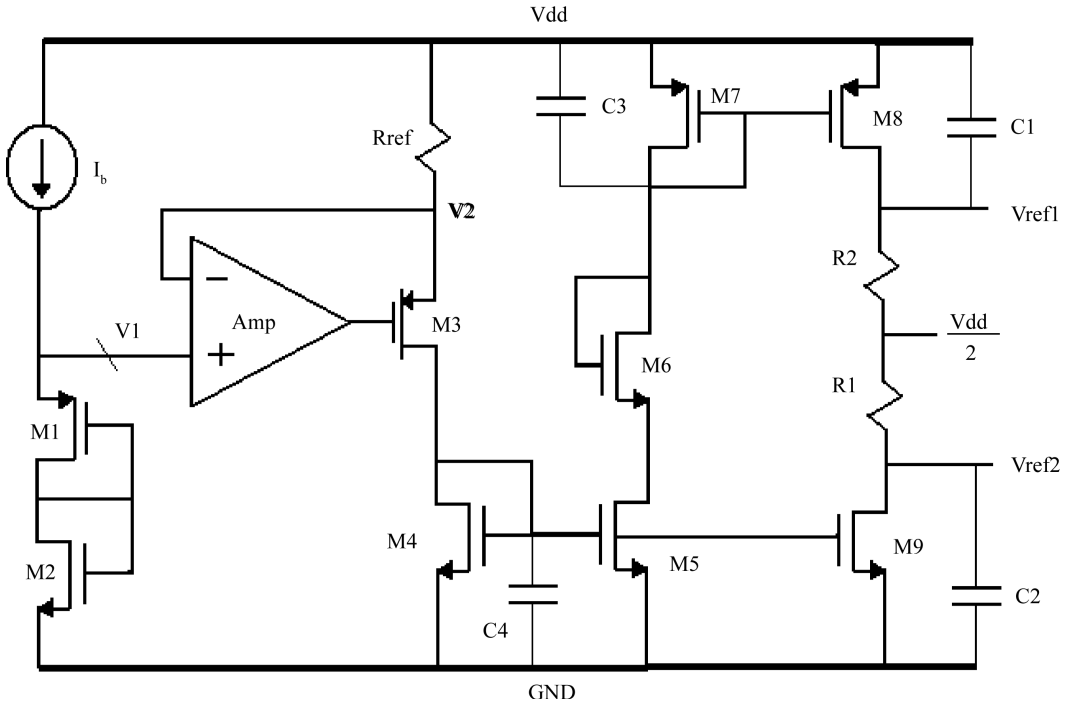


Figure 10. Reference voltages (Vref1, Vref2) generator circuit for input stage common-mode feedback circuit.

fixed to a great extent and temperature increase cannot change the bias current of output devices.

The same concept occurs when the temperature decreases. Temperature reduction decreases the bias current of output devices. And the same decrease occurs in the bias current of M1 and M2 devices. So the voltage dc-shift between the gates of output stage devices decreases using circuit of **Figure 10**. Hence the bias currents in these devices remain constant. As mentioned before this circuit (circuit of **Figure 10**) minimizes the effect of temperature variation on the performance of LD by providing a negative feedback process to adjust the bias current of the output stage devices. Although the temperature variations can change the threshold voltage of the other transistors in the circuit (e.g. first stage's devices and M3-M9 in the circuit of **Figure 10**), most of them are current mirror devices and so the temperature variations cannot influence the bias currents of them significantly.

This circuit can compensate the power supply noise effect on the LD. Although the designed LD is a fully differential circuit and can eliminates common-mode type noises such as power supply noise, any mismatch between the devices of two parts of the differential output stage of LD causes to remain a portion of the power supply noise in the output voltage of the LD. This degrades the THD and the performance of the LD. So reducing the effect of power supply noise on the each sides of the LD improves the performance of the LD. Power supply noise directly changes the Vgs of the output devices because the source of these devices is connected to Vdd and GND. To compensate this effect the gate voltage of these devices must be changed with supply noise in order to keep the Vgs of the output stage devices constant. To change the gate voltages of these devices, some capacitors (c1-c4) are added to the circuit of **Figure 10**. These capacitors apply the power supply noise to the Vref1 and Vref2 nodes. Also the common mode feedback circuits of the first stage transfers the power supply noise from Vref1 and Vref2 to the gates of the output stage devices. Therefore the power supply noise cannot change the Vgs of the output stage devices to a great extent. So the significant portion of the noise caused by the power supply noise in the output voltages of the LD is reduced by using this technique and the PSRR of the LD improves.

Furthermore the process variation cannot change the value of the dc-shift voltage and bias current of output devices. The resistors (R1, R2) in the circuit of **Figure 10** provide a dc shift between the gates of output devices. The value of resistors might change due to the process variations up to 20%. This can cause considerable change in the bias current of output devices. In order to reduce the effect of resistance variation, the current of these resistors are changed in the opposite direction such that the dc voltage across the resistors remains constant. In this

circuit a reference current which is sensitive to the resistance variation is produced and mirrored to the M8 and M9 devices and passes from R1 and R2 resistors. The reference current is:

$$I_{ref} = \frac{(V_{dd} - V_2)}{R_{ref}} \tag{28}$$

The process variation cause an approximately equal change in the value of resistors (R_1, R_2, R_{ref}) in the circuit of **Figure 10**, so the dc shift (Vref1-Vref2) remains constant to a great extent. The op-amp used in the circuit of **Figure 10** is a simple single stage amplifier with very low bias currents to minimize the power consumption.

3. Controller Design

Figure 11 shows the simplified block diagram of the designed adaptive LD. As mentioned before in the proposed LD impedance matching is done using a topology wherein, when the output voltage is equal to the input, the output resistance is matched to the line [1] [8]. The interface block shown in **Figure 11**, consists of peak detector and differentiator circuits. The peak detector circuits are used to extract the peak voltages of the output nodes (V_o^+, V_{out}^+). The voltage peak detector circuit is shown in **Figure 12**. In this circuit the capacitors charge with larger currents, proportional to the voltage of V_o^+ and V_{out}^+, but discharges with lower currents which are the bias currents of the Mp3 and Mp4 devices (Notice that the capacitors discharge when the voltage of the output nodes goes down). Therefore these circuits can detect the peak voltages of the output nodes (V_o^+, V_{out}^+) with a voltage dc-shift. This dc-shift has a negligible effect on the performance of the controller, because the difference of peak voltages is important in the impedance matching process. First input of the FLC is the difference of positive peak voltages of V_o^+ and V_{out}^+ (**e**). Another input of FLC, is the variation of the **e** (Δ**e**). The differentiator circuit has a simple structure that is not discussed in this paper.

The complete block diagram of the used neuro-fuzzy controller is shown in **Figure 13**. This FLC is based on ANFIS architecture [3] that can easily provide a mapping between stipulated input/output data pairs. The proposed controller is investigated in detail in [4]. By applying some changes to [4], it has been used to control the output impedance and the gain of the LD. The modified controller has 2 inputs, 9 rules, and 9 singletons. Each input has bell-shape membership functions with 4 bit digital input, to control its slope. The characteristics of the membership functions (slope and position) can be tuned by using learning algorithm [4] to reduce the total error

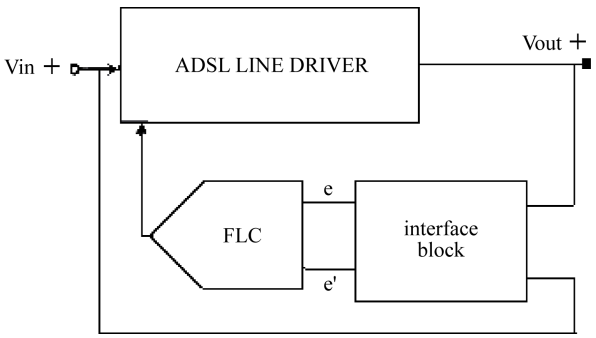


Figure 11. System block diagram of the adaptive LD.

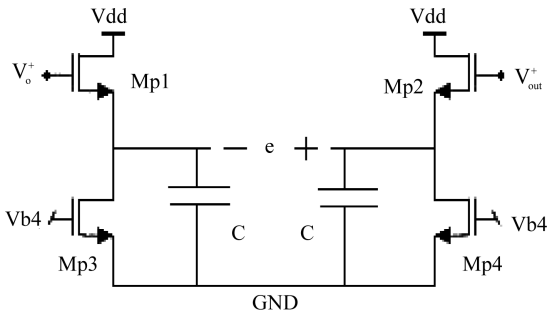


Figure 12. Peak detector circuit.

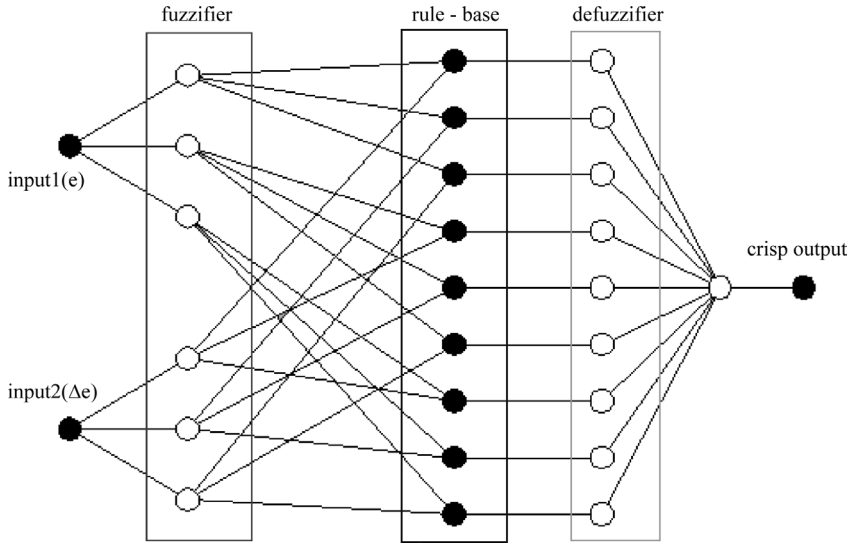


Figure 13. Block diagram of the neuro-fuzzy controller.

Table 2. Employed rule base.

Δe \ e	N	Z	P
N	*P*	*P*	*Z*
Z	*P*	*Z*	*N*
P	*Z*	*N*	*N*

of the mapping. All blocks of the FLC (except the fuzzifier block) are in current mode, so the controller is simple. Each block has high accuracy, low power consumption, and small occupied area [4]. By using modified ANFIS architecture, in the defuzzifier block the divider circuit has removed [4], therefore the occupied area and power consumption of FLC has reduced. Transistor level circuit of each layer is described in [4].

Inference Engine and Rules

Each input **e** and **Δe** has three membership functions labeled Negative (**N**), Zero (**Z**), and Positive (**P**) that provide 9 rules. From **Table 2**:

Rule1: If **e** is **N** and **Δe** is **N** then out is **P**.
Rule2: If **e** is **N** and **Δe** is **Z** then out is **P**.
Rule3: If **e** is **N** and **Δe** is **P** then out is **P**.
...
Rule9: If **e** is **P** and **Δe** is **P** then out is **N**.

4. Simulation Results

In this section, the simulation results of the proposed LD are shown and the proposed LD is compared with the some conventional LDs. The proposed LD has been designed in a typical 0.35 μm CMOS process and is simulated by HSPICE software using *level* 49 parameters (BSIM3v3). Transient response and Ac response of the LD are shown for a constant load (RL = 75 Ω, CL = 10 pF) in **Figure 14** and **Figure 15**. **Figure 14(b)** shows a 3.2 V_{p-p} output waveform of the LD. The LD drives a 75 ohms resistive load and 10 pF single-ended capacitors which include pad capacitors. The closed-loop and open-loop frequency response of the LD while driving a 75 Ω and 10 pF output capacitors are shown in **Figure 15** and **Figure 16** respectively. Output spectrum (FFT analysis) for the same test is shown in **Figure 17**. It shows about −67 dB THD. To simulate the effect of the power supply noise in the LD and evaluate the performance of the circuit of **Figure 10** in compensating the power supply noise, some sinusoidal voltage sources with different frequencies are added in series with the Vdd. **Figure 18** shows the efficiency of the employed technique in the improving the PSRR. In fact the negative effect of

the power supply noise in the THD of LD is reduced to a great extent by using this circuit. **Table 3** summarizes the THD of the LD in the different RL and different frequencies in 3.2 Vp-p output voltage swings. **Table 4** summarizes the THD of the LD in the different output voltage swings. **Table 5** summarizes the main features of this design and compares it with some recent works. It shows that bandwidth, power consumption and especially THD performance, are considerably improved compared to the other designs. To show the performance of the FLC, error (**e**) and change of error (**Δe**) signals are applied to the FLC. Also a differential 90 Ω load is connected to the output nodes of the LD. As shown in **Figure 18** termination (e ≈ 0) has been done by FLC in about 28 usec. After 110 usec the load resistor (RL) is changed to 75 Ω. In this case the impedance termination has been done in about 15 usec. The simulation result of the impedance termination is shown in **Figure 19**.

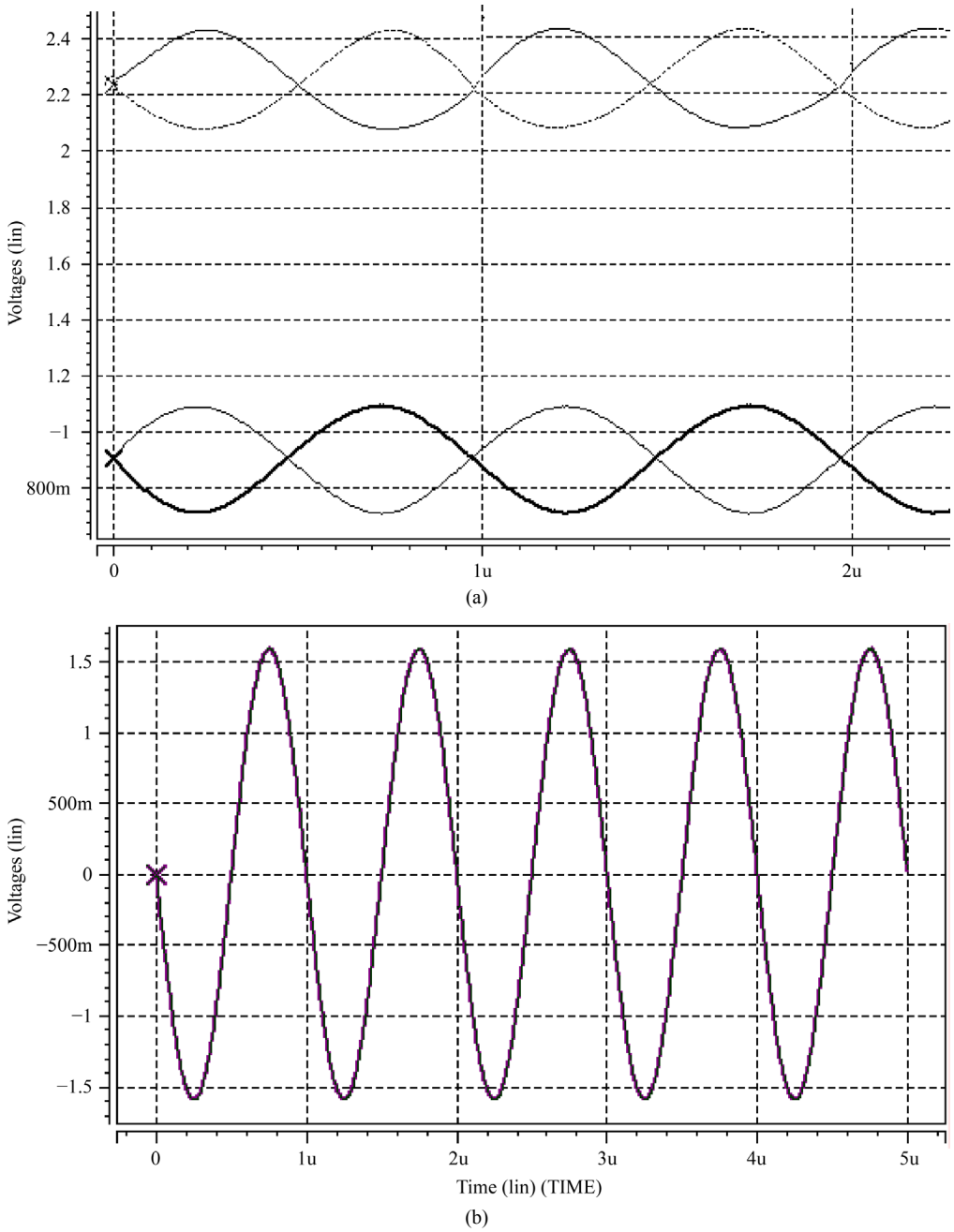


Figure 14. (a) Preamplifier output waveform (b) A 3.2 Vp-p output waveform of the LD while driving a 75 Ω and 10 pF load at 1 MHz.

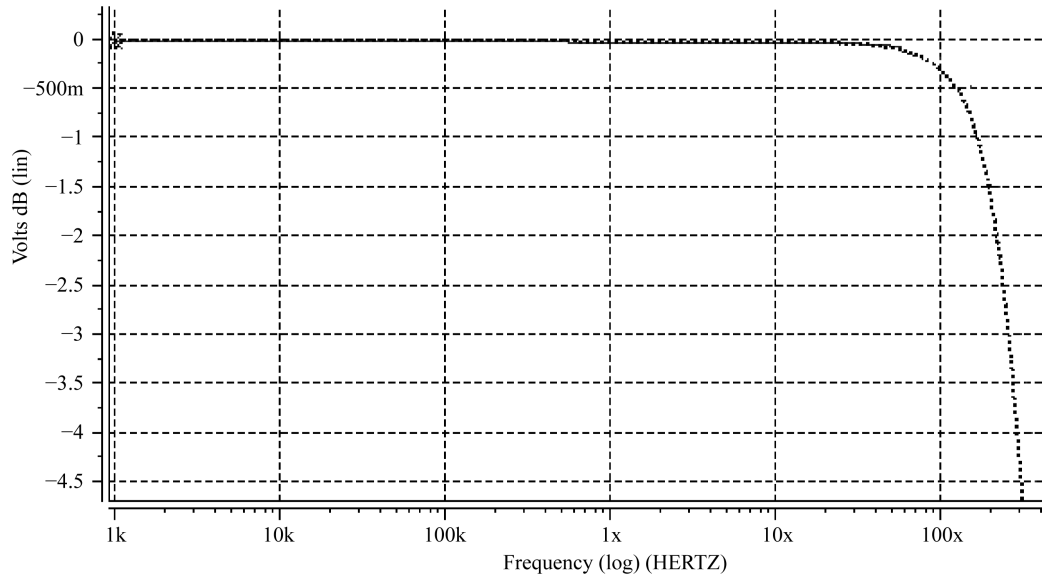


Figure 15. Closed-loop frequency response of the output of the LD driving a 75 Ω and 10 pF load (Magnitude).

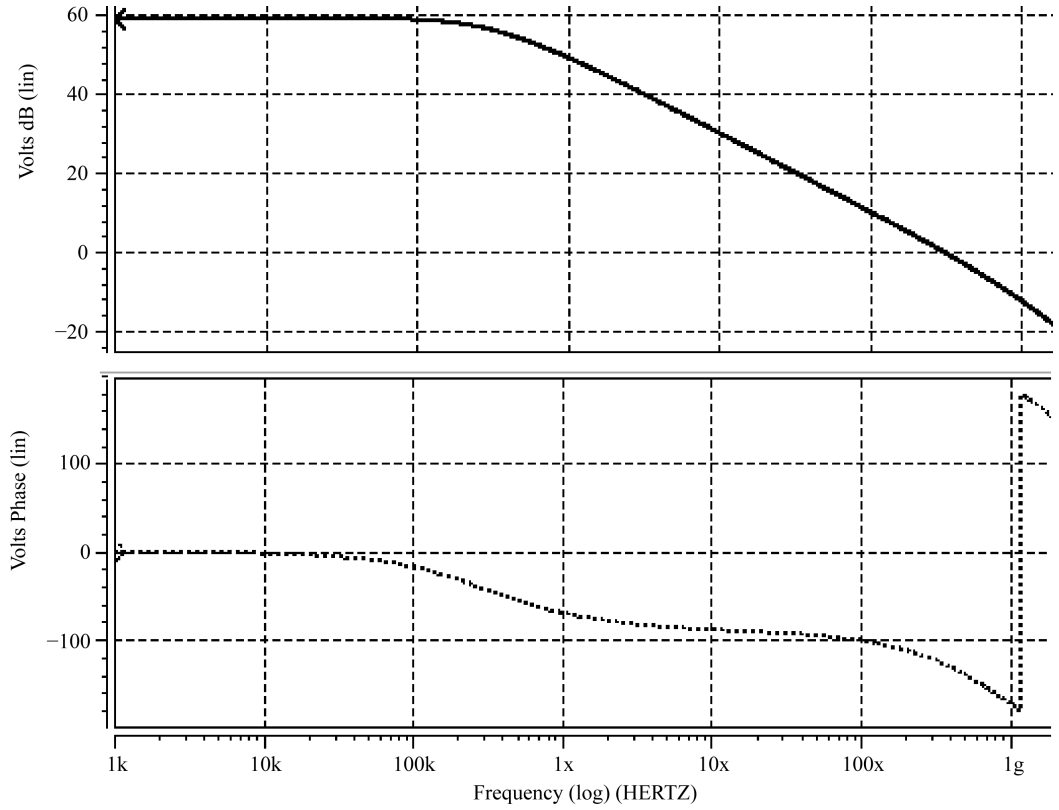


Figure 16. Open-loop magnitude and phase of the LD output while driving a 75 Ω and 10 pF load.

5. Conclusion

A differential adaptive LD suitable for ADSL modems with 240-MHz bandwidth and better than 67 dB total harmonic distortion, has been presented. Also in this structure a novel application for fuzzy logic controller is introduced. This topology addresses some of the requirements of modern transceivers by providing integrated

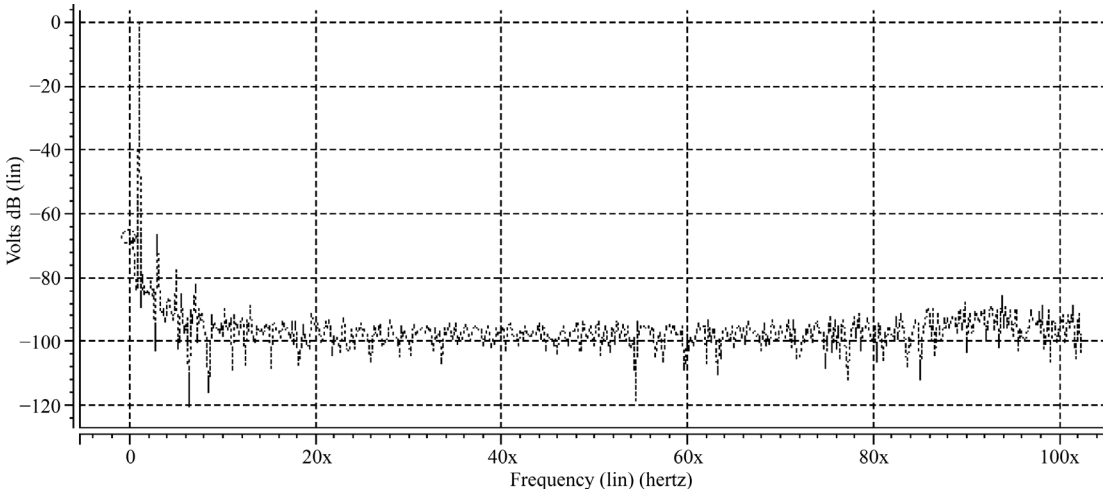
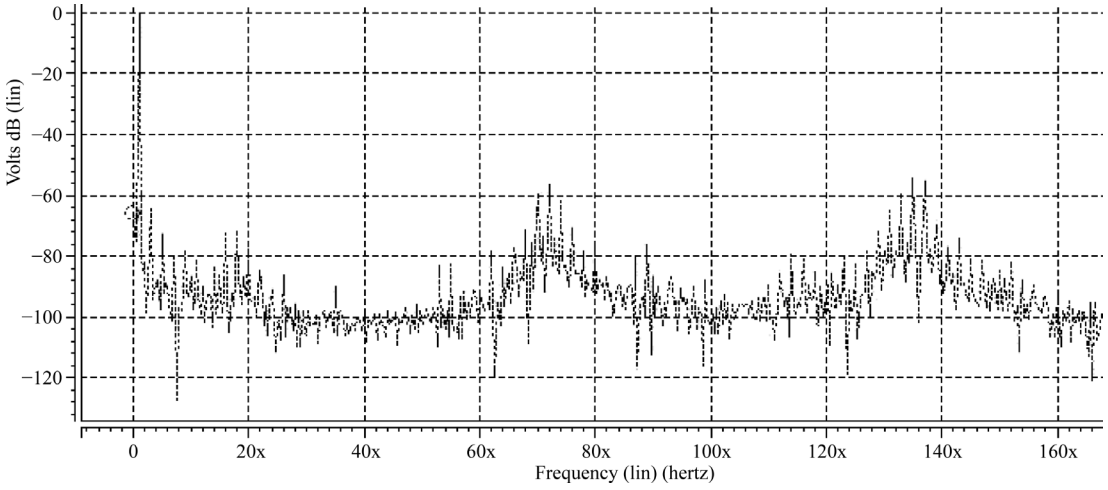
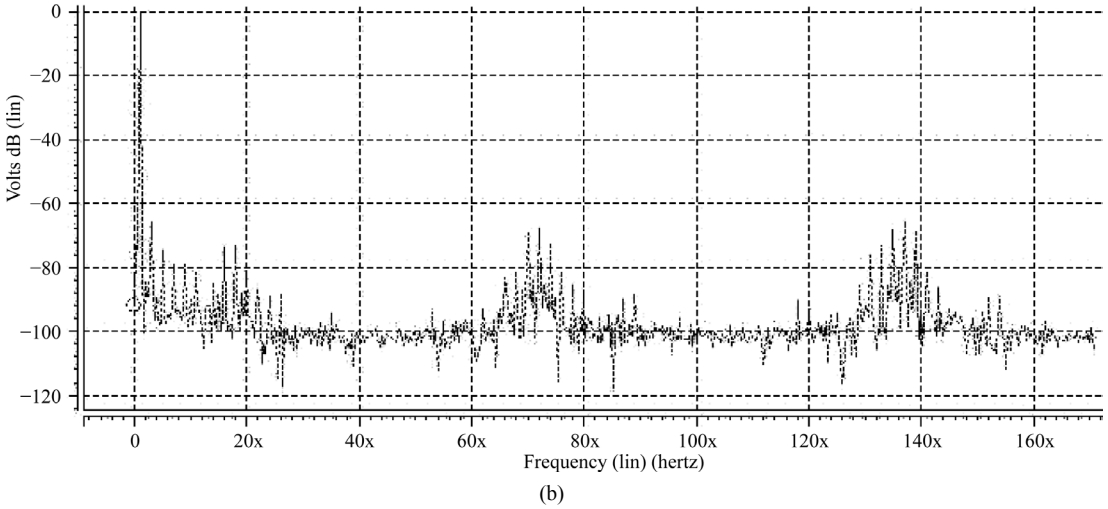


Figure 17. A 3.2 VP-P output spectrum of the LD while driving a 75 Ω and CL = 10 pF load at 1 MHz.



(a)



(b)

Figure 18. Effect of the supply noise on the output spectrum of the LD while driving a 75 Ω and CL = 10 pF load at 1 MHz and 3.2Vp-p amplitude. (a) Without compensator capacitors in the circuit of **Figure 10**. (b) Output spectrum with compensator capacitors.

Table 3. THD in different RL and different frequencies.

Fin	100 KHz	300 KHz	500 KHZ	800 KHz	1 MHz
***RL*= 60**	80 dB	77 dB	72 dB	70 dB	63 dB
***RL* = 75**	84 dB	80 dB	76 dB	73 dB	67 dB
***RL* = 90**	86 dB	82 dB	78 dB	75 dB	70 dB

Table 4. THD in different output voltage swings (Rl = 75, Fin = 1 Mhz).

***Output swing* (*v*)**	3.2	3	2.7	2.5
THD	67 dB	72 dB	77 dB	86 dB

Table 5. Circuit characteristic and comparison.

Parameters	**This work**	**[6]**	**[1]**	**[8]**
Power supply	3.3 V	3.3 V	3.3 V	3.3 V
Technology (μm)	0.35	0.35	0.35	0.5
Power dissipation (mW)	107	140	155	-
Load range	60 - 90 Ω	-	60 - 90 Ω	70 – 180 Ω
−3dB Freq (MHz)	240	261	160	15
THD (dB)	−62 3.2 Vpp 5 MHz	−74.5 3.3 Vpp 10 MHz	−47.5 2 Vpp 10 MHz	−45 1.2 Vpp 5 MHz
Maximum output voltage swing (v)	3.8	3.8	2	1.6
Adaptive	*yes*	*no*	*yes*	*yes*

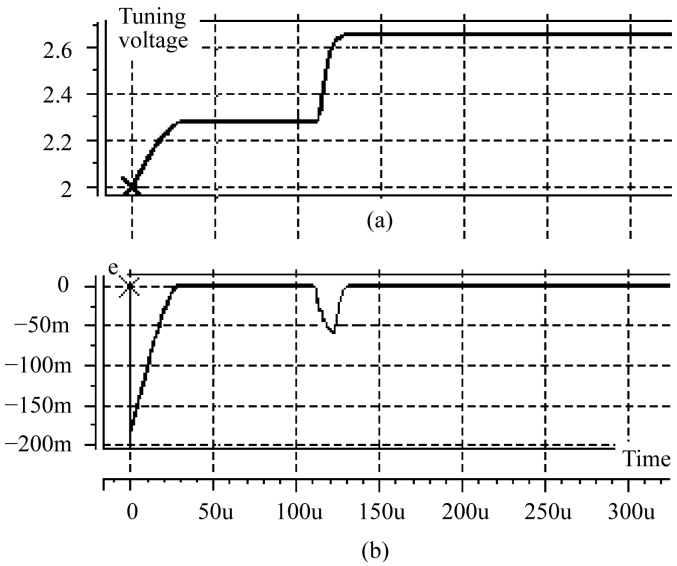


Figure 19. Simulation result of the structure for cable impedance variations (90 to 75 ohm). (a) Output of FLC (b) Error voltage (e).

termination without incurring signal loss. Because of using fully differential architecture, common-mode disturbances, such as substrate or power supply noise are cancelled to a great extent. Also a novel technique is used to minimize the effects of temperature and process variations. Furthermore, PSRR of LD is improved in comparison with other works. In addition, even order harmonics are also eliminated. Due to the presence of the automatic tuning loop, it provides robust performance regardless of load variations. These performance improvements have been achieved at the cost of increased complexity of the driver.

References

[1] Mahadevan, R. and Johns, D.A. (2000) A Differential 160-MHz Self-Terminating Adaptive CMOS Line Driver. *IEEE Journal of Solid-State Circuits*, **5**, 1889-1894. http://dx.doi.org/10.1109/4.890302

[2] Jang, J. (1993) ANFIS: Adaptive-Network-Based Fuzzy Inference System. *IEEE Transactions on Systems*, *Man*, *and Cybernetics*, **23**, 665-685. http://dx.doi.org/10.1109/21.256541

[3] Peymanfar, A., Khoei, A. and Hadidi, Kh. (2007) A New ANFIS Based Learning Algorithm for CMOS Neuro-Fuzzy Controllers. *The* 14*th IEEE International Conference on Electronics*, *Circuits and Systems*, Marrakech, 11-14 December 2007, 890-893. http://dx.doi.org/10.1109/icecs.2007.4511134

[4] Peymanfar, A., Khoei, A. and Hadidi, Kh. (2009) Design of a General Propose Neuro-Fuzzy Controller by Using Modified Adaptive-Network-Based Fuzzy Inference System. *International Journal of Electronics and Communications*, **60**, 557-566.

[5] Hadidi, Kh., Oshima, H., Sasaki, M. and Matsumoto, T. (2002) A Highly Linear Fully Differential Low Power CMOS Line Driver. *Proceeding of Europe Solid-State Circuits Conference*, Portugal.

[6] Oskooei, M.S., Hadidi, K. and Khoei, A. (2005) A Highly Linear and Large Bandwidth Fully Differential CMOS Line Driver Suitable for High-Speed Data Transmission Applications. *IEICE Transactions on Fundamentals of Electronics and Computer Sciences*, **E88-A**, 416-423. http://dx.doi.org/10.1093/ietfec/E88-A.2.416

[7] Razavi, B. (2001) Design of Analog CMOS Integrated Circuits. McGraw-Hill, Boston.

[8] Prasad, N., Dinç, H. and Aydin, K. (2003) A 3.3-V CMOS Adaptive Analog Video Line Driver with Low Distortion Performance. *IEEE Journal of Solid-State Circuits*, **38**.