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Implementation & Comparative Analysis of 10, 18 & 24 Level Diode Clamped Inverters Using "Trust Region Dog Leg" Method

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Abstract

Multilevel inverters are used in many industrial applications because of good power quality, minimum losses and less harmonics contents. Multilevel inverters require no series connected synchronized switching devices, transformer and complex filters. In this paper 10, 18, 24 diode clamped multi-level inverters (DCMLI) are implemented using trust region dog leg optimization method to find the optimized values of switching angles (θ). It decreases the total harmonic distortion (THD) of the output voltages and to reduce the complexity of external filter required. The multi-level inverters are implemented in MATLAB Simulation and results are compared in terms of harmonics, system complexity and efficiency.

Keywords

DCMLI, THD, Switching Angles, IGBTs, Trust Region Dog Leg

1. Introduction

Different techniques like Sinusoidal pulse width modulation (SPWM), SVPWM and multilevel inverters are used for the conversion of DC into AC power [1]. Numerous techniques of multi-level inverters are implemented to improve the power quality and harmonic distortion [2]. 5-level cascaded multi-level inverter implemented for power quality improvement using DSTATCOM with isolated energy for DC storage [3]. A chopper circuit with the flying capacitor voltage diode clamped for alignment of multilevel inverters reduces chopper frequency and voltage to AC voltage multilevel production [4]. 5-level diode clamped inverter for electric ma-

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chines, working at high speed with the power of twelve [5]. 3-level diode clamped inverter with active neutral points and zero current transition (3 tests such as pre-employment) use it for sustainable energy [6].

Comparison between two diodes clamped inverter nerve point of converter (DNPC-3 l tests such as pre-employment) and (ANPC-3 l tests such as pre-employment) discussed options for switching energy volume [7]. Using capacitors and one DC source to build multilevel inverter cascaded (H-bridge) [8].

H-bridge multilevel inverter flying capacitor using two different schemes of voltage balancing and equations used [9]. The closed method based on carrier to minimize losses of switches for a half cycle of the basic wave is used for analyzing each half-cycle of the switch area [10]. Two SVM methods are executed that explosive for the purpose of controlling the DVR in order to reduce the losses in the circuit breakers and less harmonic DIS [11]. Particle Swarm Optimization used in cascade inverter to reduce harmonics improve output quality [12]. Cascade multilevel inverter is implemented by using the theory of vector space to switch strategies in the topology. The proposed topology reduces harmonic distortion and switching frequency employed switches [13].

This proposed converter, diodes clamped multilevel inverters (DCMLI) for different levels of switching angles are calculated using the dog leg in order to minimize the total harmonic distortion (THD), improve the quality of the electricity voltage wave form, the overall efficiency of the inverter, as well as to study the relations of levels with THD.

2. Methodology

Circuit diagrams of diode clamped multilevel inverters (DCMLI) 10, 18, 24 levels are shown in the **Figures 1-3** respectively. DCMLI consists of two legs and each leg consists of two sub-systems connected in series. Each subsystem comprises $(m/2-1)$ switches. Every level of multilevel inverter has its own requirement of numbers of switches (IGBTs), batteries and clamping diodes. The components are calculated using Equations (1), (2) and (3) and shown in **Table 1**.

$$\text{No. of switches}(\text{IGBTs}) = 4(m/2-1) \tag{1}$$

$$\text{No. of batteries} = (m/2-1)(2) \tag{2}$$

$$\text{No. of diodes} = (m/2-1)(m/2-2) \tag{3}$$

Switches of subsystem 1 are connected in series with subsystem 2 in one leg and similarly subsystem 3 with subsystem 4 in other leg. The output of the DCMLI is stepped stair case voltage levels as shown in **Figure 5** for 10 levels DCMLI. To obtain different voltage levels and to eliminate lower order harmonics such as 3rd, 5th, 7th, 11th and 13th, selective harmonic elimination technique is implemented using Trust Region Dog Leg, the flow diagram is shown in **Figure 4**. Dogleg utilizes Newton and steepest descent methods. The combination of these

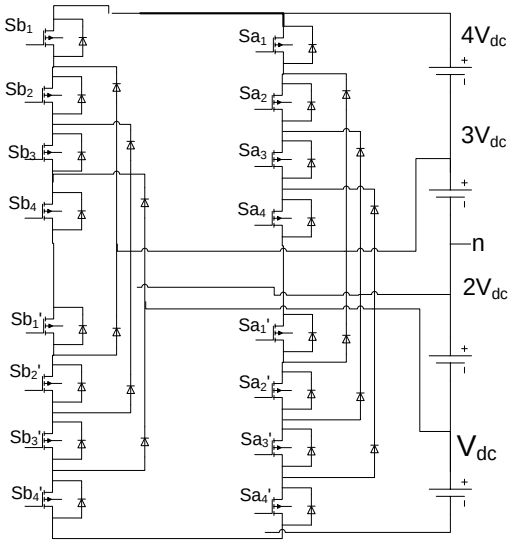

Figure 1. 10 level DCMLI.

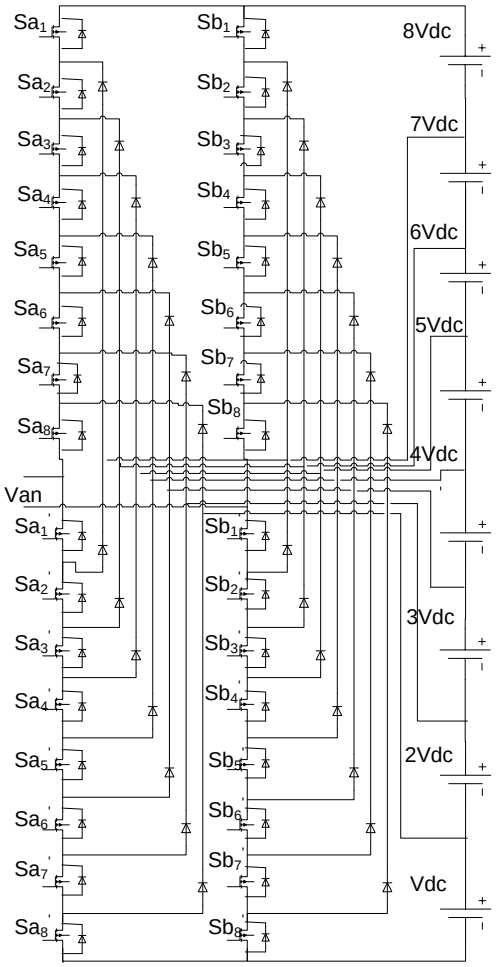

Figure 2. 18 level DCMLI.

Table 1. Number of components required for DCMLI.

DCMLI	Number of switches	Number of batteries	Number of diodes
10 level	16	4	12
18 level	32	8	56
24 level	44	11	110

two methods ensures a fast convergence and a solution of function in the steepest descent direction. The second step involves finding the value of trust region radius to estimate length of step for the current iteration such that the following condition is obeyed. Trust region dog leg optimization technique is utilized to find out the optimized switching angles using a set of non-linear equations derived to selectively eliminate specific harmonics (Selective Harmonic Elimination). The set of non-linear equations are shown in Equations (14), (15) and (16) and trust region dog leg method determines the optimized switching angles to result a wave form with minimum Total Harmonic Distortion (THD).

For particular switching angle different switches are turned on, for 10 levels four switches and 8 for 18 levels and 11 for 24 levels are on in one leg and 4, 8 and 11 in another leg. Every switch is turned on and off only once in half cycle therefore the switching losses are low. **Table 2** is showing the switching states for one leg 10 levels DCMLI.

For positive cycle all switches of subsystem 3 are OFF and sub system 4 are ON. For negative cycle, switches

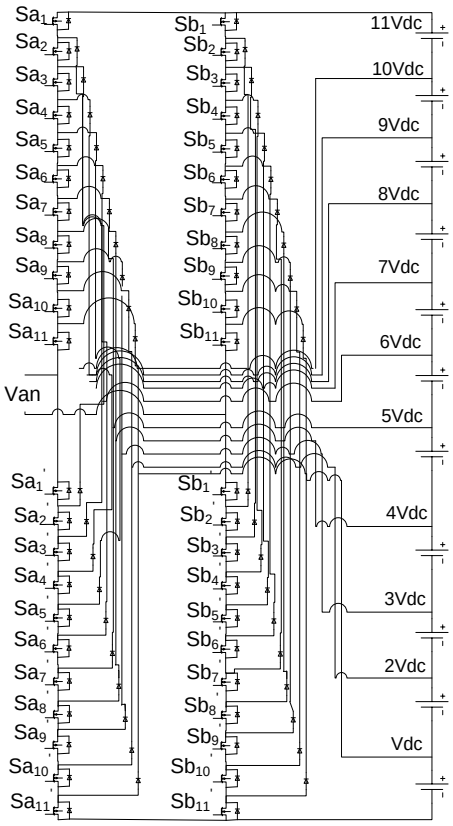

Figure 3. 24 level DCMLI.

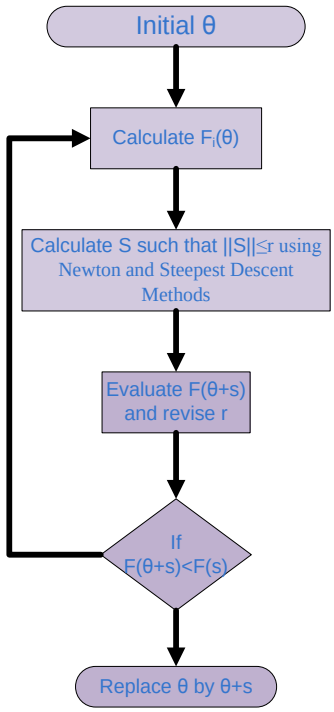

Figure 4. Trust region dogleg flow diagram.

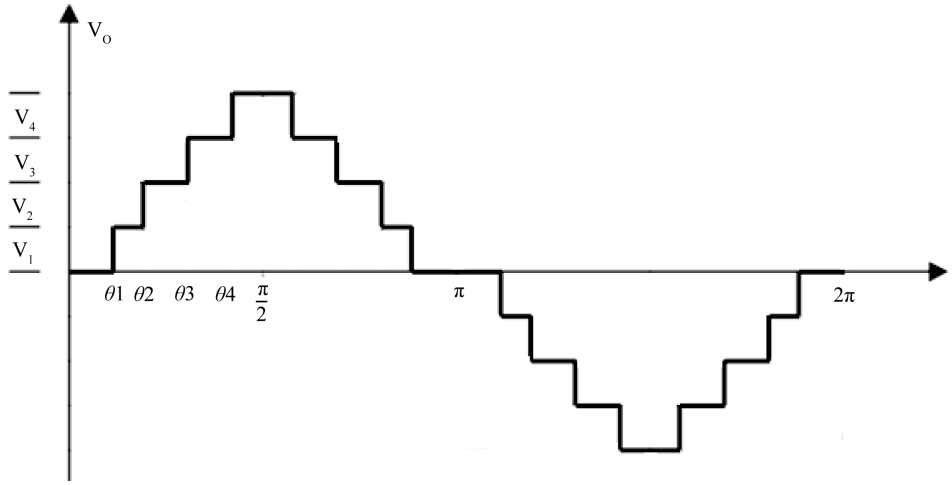

Figure 5. Output of 10 levels DCMLI.

Table 2. On-off switching pattern for 10 Level DCMLI.

Output v_{out}	Switches state of first leg for positive half cycle of 10 levels DCMLI							
	s_{a1}	s_{a2}	s_{a3}	s_{a4}	s'_a	s'_{a2}	s'_{a3}	s'_{a4}
$v_4 = 4v_{dc}$	1	1	1	1	0	0	0	0
$v_3 = 3v_{dc}$	0	1	1	1	1	0	0	0
$v_2 = 2v_{dc}$	0	0	1	1	1	1	0	0
$v_1 = v_{dc}$	0	0	0	1	1	1	1	0
$V_0 = 0$	0	0	0	0	1	1	1	1

of subsystem 3 and subsystem 4 are ON and OFF in the similar way and all switches of sub system 1 are OFF and subsystem's 2 are ON. Similarly switching states of 18 and 24 levels are shown in **Table 3**, **Table 4**.

As shown in **Figure 5** each half cycle of the output voltage is divided into multi-levels for optimized switching angles (θ). The switching angles are determined using Fourier series to find system of non-linear equations and further "trust region dogleg" method is applied. Fourier series is applied first to find out a set of non-linear equations.

From Fourier series the periodic function can be expressed as following

$$f_t = a_v + \sum_{n=1}^{\infty} a_n \cos\left(2\pi n f_o t\right) + b_n \sin\left(2\pi n f_o t\right) \quad n = 1, 2, 3, \cdots, \infty \tag{4}$$

a_v, a_n and b_n are Fourier coefficient and can be determined from following equations

$$a_v = \frac{1}{T}\int_{t_o}^{t_o+T} f(t)\,\mathrm{d}t \tag{5}$$

$$a_n = \frac{2}{T}\int_{t_o}^{t_o+T} f(t)\cos\left(2\pi n f_o t\right)\mathrm{d}t \tag{6}$$

$$b_n = \frac{2}{T}\int_{t_o}^{t_o+T} f(t)\sin\left(2\pi n f_o t\right)\mathrm{d}t. \tag{7}$$

Here T is the fundamental period and t_o is arbitrary reference time.

Multi-level inverters have odd quarter wave symmetry so they posse both odd and half wave symmetry. The Fourier coefficient for odd quarter wave symmetry simplifies to

Table 3. Switching states of 18 levels DCMLI.

Output v_{out}	Switches state of first leg for positive half cycle of 18 level DCMLI															
	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	s_1'	s_2'	s_3'	s_4'	s_5'	s_6'	s_7'	s_8'
$8v_{dc}$	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
$7v_{dc}$	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
$6v_{dc}$	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
$5v_{dc}$	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
$4v_{dc}$	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
$3v_{dc}$	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0
$2v_{dc}$	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0
v_{dc}	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Table 4. Switches state of both legs of 24 levels DCMLI.

	Switches state of 24 level DCMLI in both legs	
	Conducting switches	Non conducting switches
$11v_{dc}$	$s_1, s_2, s_3, \cdots, s_{11}, s_{34}, s_{35}, s_{36}, \cdots, s_{44}$	$s_{12}, s_{13}, s_{14}, \cdots, s_{33}$
$10v_{dc}$	$s_2, s_3, s_4, \cdots, s_{12}, s_{34}, s_{35}, s_{36}, \cdots, s_{44}$	$s_1, s_{13}, s_{14}s_{15}, \cdots, s_{33}$
.		.
.		.
.		.
v_{dc}	$s_{11}, s_{12}, s_{13}, \cdots, s_{21}, s_{34}, s_{35}, s_{36}, \cdots, s_{44}$	$s_1, s_2, s_3, \cdots, s_{10}, s_{22}, s_{23}, s_{24}, \cdots, s_{33}$
0	$s_{12}, s_{13}, s_{14}, \cdots, s_{22}, s_{34}, s_{35}, s_{36}, \cdots, s_{44}$	$s_1, s_2, s_3, \cdots, s_{11}, s_{23}, s_{24}, s_{25}, \cdots, s_{33}$

$s_1, s_2, s_3, \cdots, s_{11}$ = subsystem 1 switches; $s_{12}, s_{13}, s_{14}, \cdots, s_{22}$ = subsystem 2 switches; $s_{23}, s_{24}, s_{25}, \cdots, s_{33}$ = subsystem 3 switches; $s_{34}, s_{35}, s_{36}, \cdots, s_{44}$ = subsystem 4 switches.

$$a_v = 0 \tag{8}$$

$$a_n = 0 \quad \text{for all } n \tag{9}$$

$$b_n = 0 \quad \text{for } n \text{ even} \tag{10}$$

$$b_n = \frac{8}{T}\int_0^{T/4} f(t)\sin(2\pi n f_o t)\,\mathrm{d}t \quad \text{for odd } n. \tag{11}$$

As $\omega t = 2\pi f_o t$, Equation (11) becomes

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} f\left(\frac{\omega t}{2\pi f_o}\right)\sin(n\omega t)\,\mathrm{d}(\omega t) \quad \text{for } n \text{ odd.} \tag{12}$$

Integrating Equation (12) W.R.T switching angles

$$b_n = \frac{4}{\pi n}v_{dc}\left[\cos(n\theta_1)+\cos(n\theta_2)+\cos(n\theta_3)+\cos(n\theta_4)+\cos(n\theta_5)\right]. \tag{13}$$

Equation (13) shows odd harmonics in DCMLI as switching angles. To eliminate 3rd, 5th, 7th, 9th, 11th and 13th harmonics and output peak voltage is controlled to *v*, harmonics equations results in

$$\frac{4}{\pi n}v_{dc}\left[\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)\right]=v \tag{14}$$

$$\left[\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)\right]=0 \tag{15}$$

$$\left[\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)\right]=0. \tag{16}$$

The values of switching angles can be calculated from these set of non-linear equations using iterative method.

Equation (14) can also be written as

$$\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)=m \tag{17}$$

where

$$m=\frac{v}{\frac{4}{\pi}v_{dc}}. \tag{18}$$

Modulation index m_a is given by

$$m_a=\frac{m}{s}=\frac{v}{\frac{4}{\pi}sv_{dc}}. \tag{19}$$

s = No. of DC sources.

The total harmonic distortion is calculated from the following equation

$$\text{THD}=\frac{\sqrt{v_2^2+v_3^2+v_4^2+\cdots+v_n^2}}{v_1} \tag{20}$$

v_2, v_3, v_n are the RMS voltage value of 2nd, 3rd and nth harmonics and v_1 is the fundamental output voltage.

Computed values of switching angles in radians of 10, 18 and 24 levels DCMLI when dog leg method is applied are **Tables 5-7**.

3. Results

Total harmonic distortion values and output voltage wave forms are observed for m = 0.9 and the variation in harmonics and the quality of output waveforms. The value of m is kept constant while total numbers of voltage levels in half cycle (0 - π) of output waveforms are increased gradually, when Voltage levels are increased the

Table 5. Switching angles of 10 levels DCMLI.

Modulation index	θ_1	θ_2	θ_3	θ_4
$m_a=0.9$	0.0942	0.3209	0.5219	0.8744

Table 6. Switching angles of 18 levels inverter.

Modulation index	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8
$m_a=0.9$	0.1359	0.2103	0.3392	0.5003	0.6483	0.9308	1.0887	1.5631

Table 7. Switching angles of 24 levels inverter.

Modulation index	θ_1	θ_2	θ_3	θ_4	θ_5	
	0.0000	0.1502	0.2408	0.359	0.491	
$m_a=0.9$	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}
	0.603	0.710	0.838	1.030	1.3253	1.5808

wave form gets closer to pure sinusoidal wave form and consequently the percent total harmonic distortion decreases. Total harmonic distortion (THD) depends on the 3rd, 5th, 7th, 9th, 11th, and 13th (in the proposed case) lower harmonics when levels are increased the harmonics results smaller peak values which decreases the THD value as shown in **Table 8** and **Figures 6-11** for various levels.

4. Conclusion

Trust region dog leg method employing optimized switching angles has reduced total harmonic distortion in multilevel inverters compared to when non-optimized switching angles are considered. It is evident from the

Table 8. THD values for DCMI.

DCMLI	% THD
10 Level	9.76
18 Level	5.91
24 Level	3.80

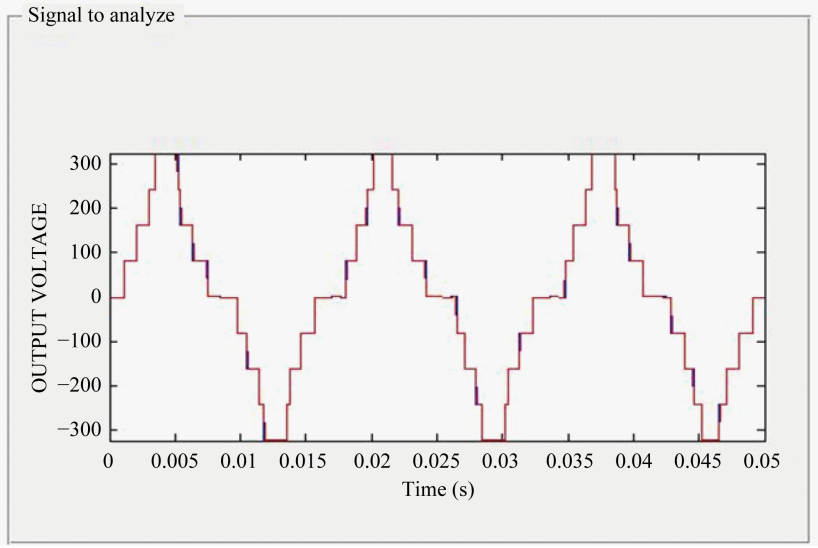

Figure 6. Output voltage of 10 levels DCMLI.

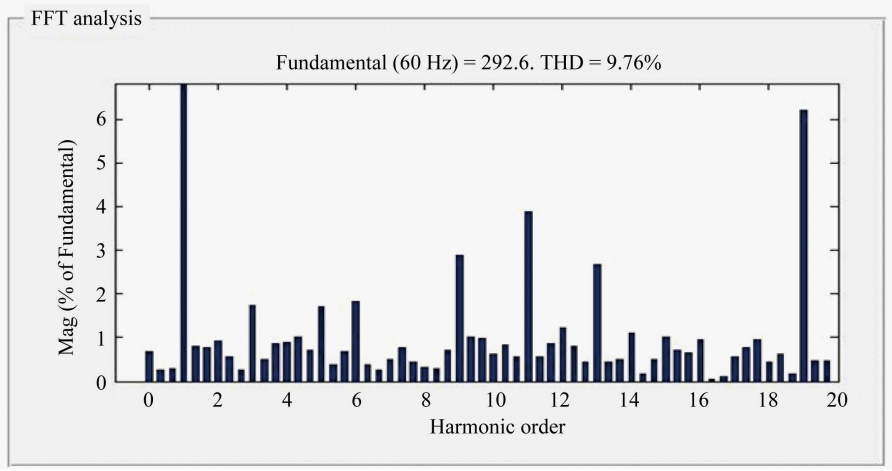

Figure 7. Frequency spectrum & THD of 10 levels DCMLI.

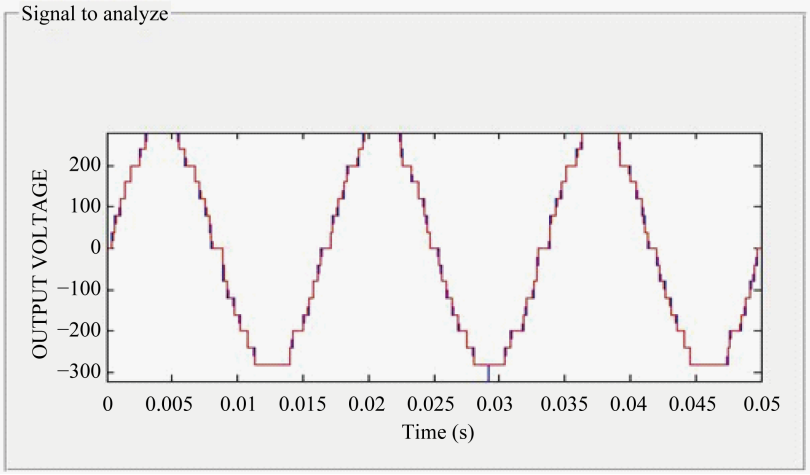

Figure 8. Output voltage of 18 levels DCMLI.

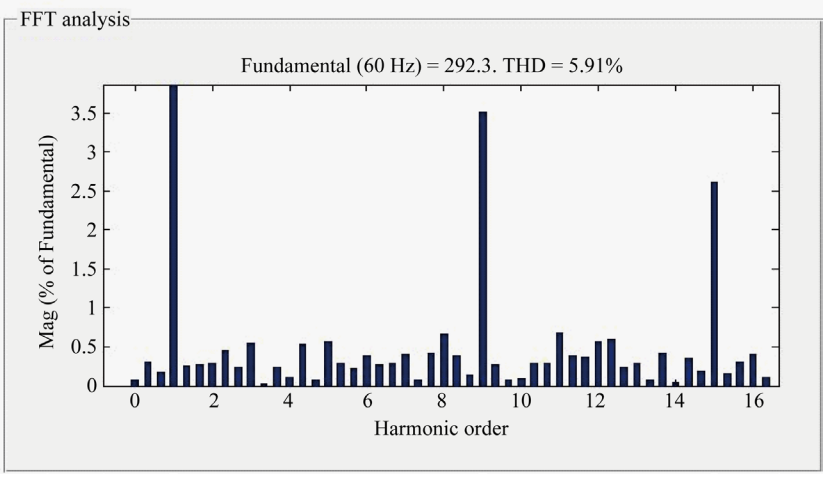

Figure 9. THD of 18 levels DCMLI.

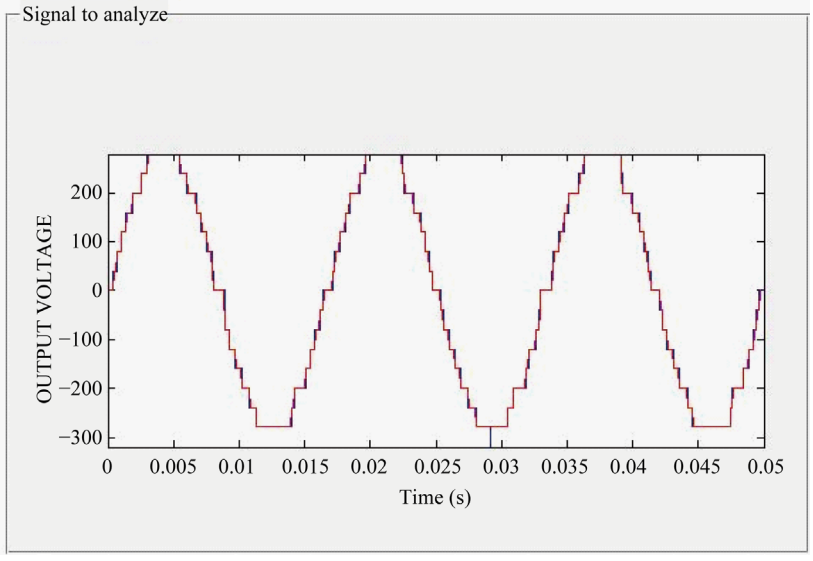

Figure 10. Output voltage of 24 levels DCMLI.

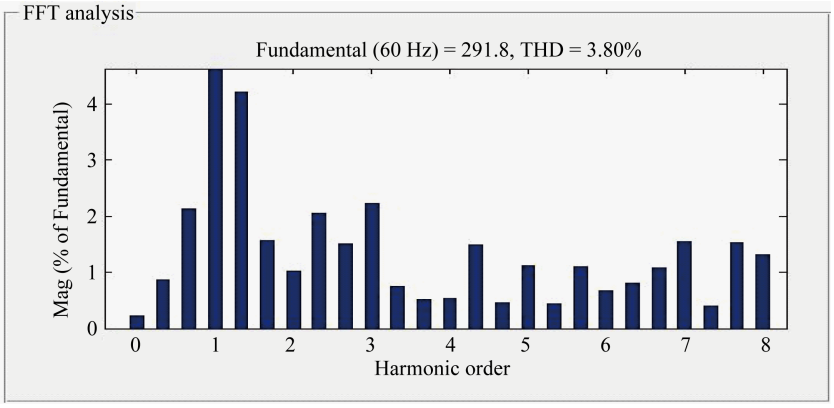

Figure 11. THD of 24 levels DCMLI.

results that an increasing number of voltage levels in the output waveforms decrease the total harmonic distortion (THD) and the output wave form gets closer to pure sinusoidal voltage plus overall efficiency of the system rises. Moreover, the number of battery sources, IGBTs and diodes required makes the system bulkier and expensive as the number of levels is increased but ensures a sooth input to the industrial load (e.g. AC Motor Drive runs with maximum torque, less noise and maximum efficiency when the higher level of multi-level inverter output is fed to it).

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