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An Improved SOI CMOS Technology Based Circuit Technique for Effective Reduction of Standby Subthreshold Leakage

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ABSTRACT

Silicon-on-insulator (SOI) CMOS technology is a very attractive option for implementing digital integrated circuits for low power applications. This paper presents migration of standby subthreshold leakage control technique from a bulk CMOS to SOI CMOS technology. An improved SOI CMOS technology based circuit technique for effective reduction of standby subthreshold leakage power dissipation is proposed in this paper. The proposed technique is validated through design and simulation of a one-bit full adder circuit at a temperature of 27˚C, supply voltage, V_{DD} of 0.90 V in 120 nm SOI CMOS technology. Existing standby subthreshold leakage control techniques in CMOS bulk technology are compared with the proposed technique in SOI CMOS technology. Both the proposed and existing techniques are also implemented in SOI CMOS technology and compared. Reduction in standby subthreshold leakage power dissipation by reduction factors of 54x and 45x foraone-bit full adder circuit was achieved using our proposed SOI CMOS technology based circuit technique in comparison with existing techniques such as MTCMOS technique and SCCMOS technique respectively in CMOS bulk technology. Dynamic power dissipation was also reduced significantly by using this proposed SOI CMOS technology based circuit technique. Standby subthreshold leakage power dissipation and dynamic power dissipation were also reduced significantly using the proposed circuit technique in comparison with other existing techniques, when all circuit techniques were implemented in SOI CMOS technology. All simulations were performed using Microwindver 3.1 EDA tool.

Keywords: Standby Subthreshold Leakage; SOI Technology; Low Power; Multi-Threshold Voltage; Stack Effect; Reverse Gate Voltage

1. Introduction

In recent years, the demand for reducing the standby subthreshold leakage power has grown significantly. This tremendous demand is mainly due to the fast growth of battery-operated portable applications such as notebook and laptop computers, personal digital assistants, cellular phones, and other portable communication devices, which remain in the standby state for a significant time interval. This leakage power dissipation is mainly noticeable in electronic portable battery operated systems having burst-mode type integrated circuits, where computation occurs for only short intervals and the system spends the majority of time in standby state [1]. Reduction of this subthreshold leakage power is highly desirable for battery operated portable systems, which remain in the standby state for the majority of their operating time.

Scaling of MOS transistors allow higher density of logic integration on a single chip. With the scaling down of MOS transistors, supply voltage has to be reduced to lower the dynamic power dissipation. The threshold voltage of the transistor has also to be scaled down to maintain the desired performance. However, reducing the threshold voltage in small geometry MOSFETs results in an exponential increase in the standby subthreshold leakage current [2]. With the scaling down in technology, recent research has shown that the subthreshold leakage current will become even greater than the dynamic current in the overall power dissipation [3]. Leakage power dissipation arises from the leakage currents flowing through the transistor when there are no input transitions

and the transistor has reached the steady state. Excessive standby subthreshold leakage power dissipation is a primary hindrance for the advancement of CMOS integrated circuits with further scaling down in technology. Suppressing subthreshold leakage current in integrated circuits is essential for achieving green computing and facilitating the proliferation of portable electronic devices. This leakage power is expected to increase 32 times per device by the year 2020 [4]. CMOS logic circuit having submicron MOSFETS involves a number of complex tradeoffs in device dimensions, which supply voltage, and the threshold voltage for minimizing this subthreshold leakage power dissipation.

Today most electronic circuits are realized using a bulk CMOS technology, which is a very mature technology. Both die size and power dissipation of electronic circuits using this bulk CMOS technology will become difficult to reduce in the future [5]. So, new advanced technologies have to be developed for reducing these emerging problems. The most promising one for ultra-low power circuit implementation is silicon-on-insulator (SOI) CMOS technology [5-7]. The ability to use a low supply voltage and to simultaneously reduce parasitic capacitances is of high importance in designing low power digital circuits [8]. Instead of a bulk silicon substrate, SOI CMOS technology employs an insulator below a thin layer of silicon which eliminates most of the parasitic capacitances found in bulk CMOS technology. This allows SOI CMOS circuits to operate with a reduced supply voltage, thus further reducing the system power consumption.

Short channel effects (SCE) such as short channel threshold voltage roll off and drain induced barrier lowering (DIBL) are becoming major challenges in deep submicron MOS transistors and circuits in CMOS technology. In order to minimize SCE, advanced MOSFET technologies have to be used. Short channel effects of MOSFETs are much less in silicon-on-insulation (SOI) technology in comparison with conventional CMOS bulk technology [9]. The main advantage of SOI technology is its reduced junction capacitance due to oxide isolation of individual circuit elements, resulting in the overall lower power dissipation. Silicon-on-insulator (SOI) technology has attracted considerable attention as a potential alternative substrate for low power application. The use of silicon-on-insulator (SOI) technology is bringing new possibilities for effective reduction of the standby subthreshold leakage power dissipation. However, the main drawback with SOI CMOS technology is its high manufacturing cost which can be prohibitive for products where low system cost is of primary concern.

Techniques such as multi-threshold CMOS (MTCMOS) technique [10,11], and super cutoff CMOS (SCCMOS) technique [12] are available in the literature for the reduction of standby subthreshold leakage power in CMOS bulk technology. In MTCMOS technique, the high V_{TH} MOS transistor can limit the down scaling of the supply voltage, V_{DD} for ultra-low power applications due to the increase in the circuit delay. The delay is influenced by the reduced effective supply voltage and use of high V_{TH} MOS transistors. The main advantage of SCCMOS technique over MTCMOS technique is the reduction in the circuit delay due to the use of low V_{TH} sleep MOS transistors. However, in SCCMOS technique, a complex controller circuit is used for providing both negative and positive gate voltages, V_{GS} to completely turn off nMOS and pMOS transistors respectively.

In this paper, an improved SOI CMOS technology based circuit technique is proposed for effective reduction of the subthreshold leakage power dissipation in standby mode. To compare the proposed technique in SOI CMOS technology with existing (MTCMOS and SCCMOS) standby subthreshold leakage control techniques in CMOS bulk technology, a one-bit full adder circuit is designed and simulated using the proposed technique. The proposed and existing techniques are also implemented in SOI CMOS technology and compared. The proposed circuit technique in SOI CMOS technology is found to dissipate the least standby subthreshold leakage power and also dynamic power dissipation is reduced significantly in comparison with other existing circuit techniques in CMOS bulk technology. Standby subthreshold leakage power dissipation and dynamic power dissipation are also reduced significantly using the proposed circuit technique in comparison with other existing techniques, when all circuit techniques are implemented in SOI CMOS technology.

The rest of the paper is organized as follows: Section 2 describes about the fundamentals and advantages of silicon-on-insulator technology for low power applications over bulk CMOS technology. Section 3 describes the subthreshold leakage power dissipation model in more details. In Section 4, a methodology for reducing the subthreshold leakage power dissipation in standby mode is discussed. Section 5 describes the proposed SOI CMOS technology based circuit technique for effective reduction of the standby subthreshold leakage power dissipation. In Section 6, simulation results are provided for a one-bit full adder circuit and the obtained results are compared using the existing circuit techniques in CMOS bulk technology and the proposed SOI CMOS technology based circuit technique. Finally, conclusion is provided in Section 7.

2. Silicon-on-Insulator CMOS Technology

Silicon-on-insulator CMOS technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor device-

manufacturing. Instead of using silicon as the substrate, as in bulk CMOS transistors, an insulating substrate can be used to improve device characteristics [13]. SOI CMOS circuits consist of single-device islands which are dielectrically isolated from each other and also from the underlying substrate. Since there are virtually no isolation constraints for individual devices, transistor and interconnect densities can be very high. In bulk CMOS devices every junction produces undesirable parasitic capacitances as well. These junction capacitances do exist in SOI CMOS devices also, but they are reduced by a factor ranging from 4 to 7 [14,15]. The main advantage of SOI technology is its reduced junction capacitance, resulting in the overall lower power dissipation.

3. Subthreshold Leakage Power Dissipation Model

Subthreshold leakage current occurs in a MOS transistor when the gate voltage, V_{GS} is below the threshold voltage of the MOS transistor. BSIM 4 subthreshold leakage current model [16] can be expressed as:

$$I_{SUB} = I_O e^{\frac{V_{GS} - V_{THO} - \eta V_{DS} + \gamma V_{BS}}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \quad (1)$$

$$I_0 = \mu C_{OX} \frac{W}{L} V_T^2 e^{1.8} \text{ and } V_T = \frac{KT}{q} \quad (2)$$

where V_{GS}, V_{DS} and V_{BS} are the gate to source, drain to source, and bulk to source voltages respectively, μ denotes the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W and L denote the channel width and channel length of the leaking MOS transistor respectively, K is the Boltzmann constant, T is the absolute temperature, q is the electrical charge of an electron, V_T is the thermal voltage, V_{THO} is the zero biased threshold voltage, γ is body effect coefficient, η denotes the drain induced barrier lowering coefficient, and n is the subthreshold swing coefficient.

In a logic circuit, the subthreshold leakage power dissipation can be calculated as the product of the number of nMOS and pMOS transistors (N_{nMOS} & N_{pMOS}), the average subthreshold leakage current per MOS transistor ($I_{SUBAVG.}$), and the supply voltage, V_{DD}. Hence it may be expressed as:

$$P_{SUB} = \left(N_{nMOS} + N_{pMOS}\right) \times I_{SUBAVG} \times V_{DD} \quad (3)$$

where $I_{SUBAVG.}$ is calculated by computing the average leakage current per MOS transistor for the given logic circuit using gate-level subthreshold leakage power estimation.

4. Methodology Adopted

Methodology for designing the proposed technique for effective reduction of the standby subthreshold leakage power is adopted after careful investigation of the subthreshold leakage current equations described in section 3.

Gate voltage, V_{GS} can be lowered by utilizing the principle of reverse gate voltage, V_{GS} to MOS transistors. There is an exponential decrease in the standby subthreshold leakage current due to the application of positive and negative gate voltages to pMOS and nMOS transistors respectively [16,17]. So, subthreshold leakage power dissipation can be reduced effectively by applying reverse gate voltages to MOS transistors.

Figure 1 [18] shows the reduction of the subthreshold leakage current due to the increase in the barrier height and the reduction in V_{DS} (= $V_{DD} - V_m$) after stacking of two cutoff nMOS transistors in comparison with a single cutoff nMOS transistor. When both nMOS transistors, Q_1 and Q_2 are turned off due to the application of $V_{GS} < V_{TH}$, then the intermediate node voltage, V_m has a positive value due to the existence of a small drain current. Thus, the gate to source voltage of Q_1 is negative, due to which the subthreshold leakage current reduces exponentially. The body effect of Q_1 (due to $V_m > 0$), further increases V_{TH} of Q_1, thereby, reduces the subthreshold leakage current. Drain induced barrier lowering (DIBL) is also reduced due to the positive value of node voltage, V_m. This increases V_{TH} of Q_2, which also contributes to the reduction of the subthreshold leakage current. Thus, the subthreshold leakage current is reduced considerably, due to stacking effect of MOS transistors.

Threshold voltage of a MOS transistor plays a vital role in low power VLSI circuit design. In the active mode of circuit operation, low V_{TH} MOS transistors are preferred for higher performance. However, for the standby mode of circuit operation, high V_{TH} MOS transistors are used for reducing the subthreshold leakage power dissipation. Hence, MTCMOS circuit technique-can be utilized for effectively reducing the standby subthreshold leakage power dissipation.

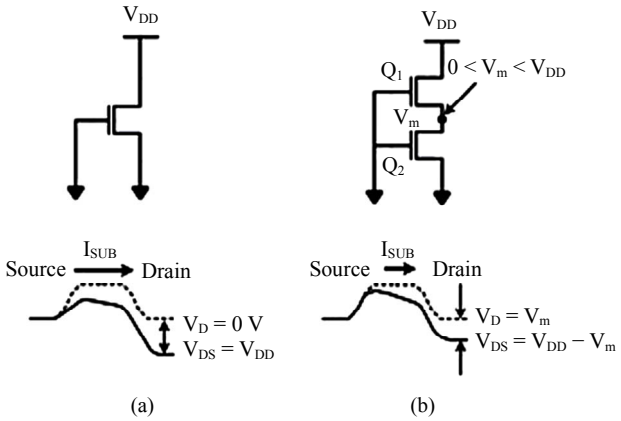

Figure 1. Standby subthreshold leakage current differences between (a) a single cutoff nMOS transistor and (b) a stack of two cutoff nMOS transistors.

Silicon-on-insulator (SOI) is a non-bulk CMOS technology. The reduction in the effective parasitic capacitance in SOI technology due to isolation from the bulk silicon makes it attractive for ultra-low power applications. The dynamic power dissipation is proportional to the total circuit capacitance and the square of the supply voltage. This means that SOI technology is very much suitable for low power operations as the parasitic capacitance is reduced and the supply voltage can be lowered. A steeper subthreshold swing helps to achieve low subthreshold leakage power dissipation.

The subthreshold swing S of a MOS transistor can be expressed as [19]:

$$S = \frac{KT\ln 10}{q}\left(1+\frac{C_{\mathrm{d}}}{C_{\mathrm{ox}}}\right) \tag{4}$$

where K is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, and C_{d} and C_{ox} are the capacitance of the depletion layer and gate oxide.

In SOI technology, $C_{\mathrm{d}}/C_{\mathrm{ox}}$ is close to zero as the depletion capacitance is negligible. An important feature in SOI technology is the steeper sub threshold slope due to a reduction in the substrate body effect. For a given $I_{\text{off-current}}$, the SOI technology has a much smaller threshold voltage, which means that the circuit can operate at a lower supply voltage. SOI technology has lower DIBL, lesser short channel effects, very good subthreshold swing, and lesser junction and parasitic capacitances in comparison with the bulk CMOS technology. Thus, the subthreshold leakage current in SOI technology is much lower than the bulk CMOS technology for the same threshold voltage.

5. Proposed Circuit Technique

The proposed circuit technique is designed after analyzing the dependence of MOS transistor parameters on the subthreshold leakage current. Methodology adopted for designing this SOI based circuit technique is discussed in detail in Section 4.

Figure 2 show salogic circuit designed using MTCMOS technique in SOI CMOS technology. This logic circuit is designed using low V_{TH} MOS transistors, and a high V_{TH}pMOS transistor is inserted between the supply voltage, V_{DD} and the logic circuit while a high V_{TH}nMOS transistor is inserted between the logic circuit and the ground. During standby mode of operation, V_{GS1} is connected to a positive gate voltage, while V_{GS2} is connected to the ground as per MTCMOS technique. **Figure 3** shows a logic circuit using the proposed SOI CMOS technology based circuit technique, which is designed from **Figure 2** after stacking high V_{TH} MOS transistors and applying reverse gate voltages, V_{GS1} and V_{GS2} (*i.e.* positive gate voltage, V_{GS1} to the stacked high V_{TH}pMOS transistors and negative gate voltage, V_{GS2} to the stacked high V_{TH}nMOS transistors) to the stacked high V_{TH}pMOS and nMOS transistors respectively in SOI CMOS technology.

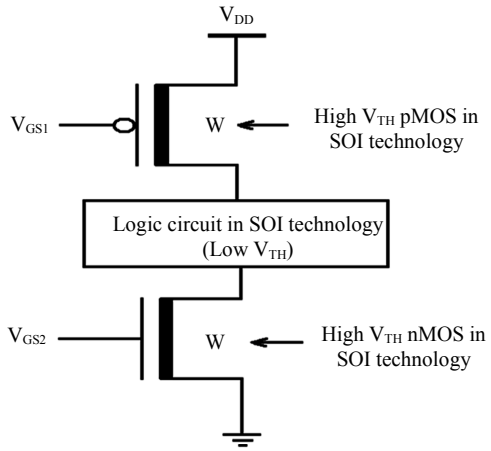

Figure 2. A logic circuit using MTCMOS techniquein SOI CMOS technology.

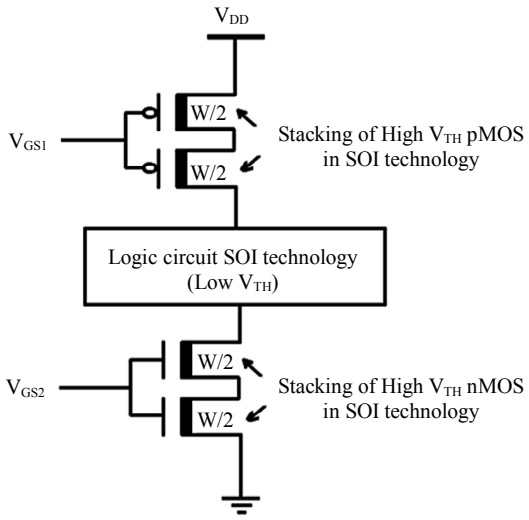

Figure 3. A logic circuit using the proposed circuit technique in SOI technology.

In this proposed technique, standby subthreshold leakage current is reduced effectively by utilizing multi-threshold MOS transistors, stacking of MOS transistors, applying reverse gate voltages, V_{GS1} and V_{GS2} (positive gate voltage, V_{GS1} to the stacked high V_{TH}pMOS transistors and negative gate voltage, V_{GS2} to the stacked high V_{TH}nMOS transistors) to MOS transistors, and using silicon-on-insulator (SOI) CMOS technology.

6. Simulation Results and Observations

Figure 4 shows the circuit diagram of a one-bit full adder using the proposed technique in SOI CMOS technology. The proposed technique in SOI CMOS technol-

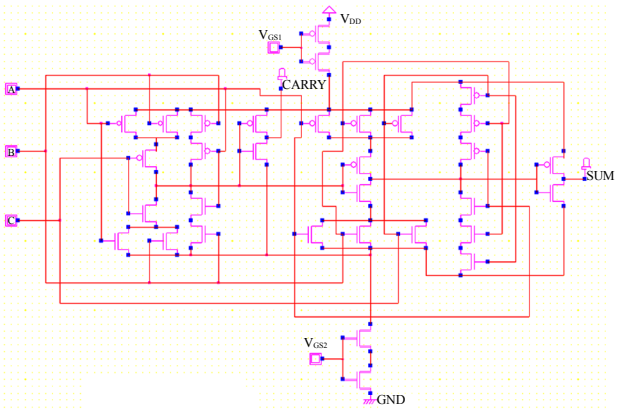

Figure 4. Circuit diagram of a one-bit full adder using the proposed technique in SOI CMOS technology.

ogy is compared with the existing techniques in CMOS bulk technology in terms of standby subthreshold leakage power dissipation, and also dynamic power dissipation. Layout of a one-bit full adder circuit was designed and simulated using Microwind ver. 3.1 EDA tool. All simulations were performed at a temperature of 27˚C and supply voltage, V_{DD} of 0.9 V in 120 nm SOI CMOS and bulk CMOS technologies. W/L of low V_{TH}nMOS and pMOS transistors were taken as 0.72 µm/0.12 µm and 1.20 µm/0.12 µm respectively. Similarly, W/L of high V_{TH}nMOS and pMOS transistors were taken as 0.72 µm/0.24 µm and 1.20 µm/0.24 µm respectively.

Standby subthreshold leakage power dissipation was measured by combining all possible input vector combinations. For calculation of standby subthreshold leakage power dissipation in a logic circuit, the voltage magnitude of all input vectors should always be less than the magnitude of the threshold voltage of the MOS transistor of the logic circuit. In this proposed technique, subthreshold leakage power dissipation in standby mode for a one bit full adder was calculated by connecting reverse gate voltages, V_{GS1} and V_{GS2} (positive gate voltage, V_{GS1} to stacked high V_{TH}pMOS transistors and negative gate voltage, V_{GS2} to stacked high V_{TH}nMOS transistors) to high V_{TH} stacked MOS transistors and applying all combinations of static input voltages, $V_{in} < V_{TH}$ to the logic circuit. Dynamic power dissipation using this proposed technique was calculated by applying input clock signals at a frequency of 5 GHz.

Standby subthreshold leakage power dissipation and standby subthreshold leakage reduction factor for a one-bit full adder circuit using the proposed technique in SOI CMOS technology in comparison with existing techniques in CMOS bulk technology are shown in **Tables 1** and **2** respectively. **Figures 5** and **6** are the graphical representations of **Tables 1** and **2** for standby subthreshold leakage power and standby subthreshold leakage reduction factor respectively. Similarly **Figures 7** and **8** are

Table 1. Standby subthreshold leakage power dissipation and dynamic power dissipation for a one-bit full adder circuit using the proposed technique in SOI CMOS technology and existing techniques in CMOS bulk technology.

References	Techniques	Standby subthreshold leakage power dissipation	Dynamic power dissipation
[10,11]	MTCMOS	0.054 nW	0.050 µW
[12]	SCCMOS	0.045 nW	0.041 µW
Proposed	Proposed	0.001 nW	0.012 µW

Table 2. Standby subthreshold leakage reduction factor and dynamic power dissipation reduction factor using the proposed technique in SOI CMOS technology in comparison with other existing techniques in CMOS bulk technology.

Techniques	Standby subthreshold leakage power dissipation	Standby subthreshold leakage reduction factor for the proposed technique in comparison to the existing techniques
Multi-threshold	0.012 nW	12x
Super cutoff	0.009 nW	9x
Proposed	0.001 nW	-

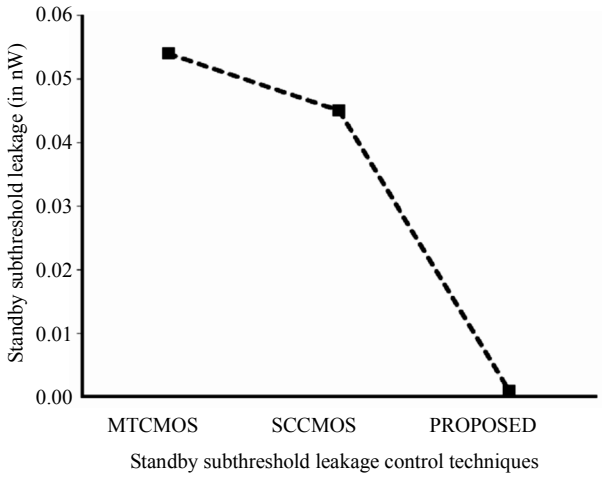

Figure 5. Standby subthreshold leakage power dissipation for a one-bit full adder circuit in MTCMOS, SCCMOS and proposed techniques.

the graphical representations of **Tables 1** and **2** for dynamic power dissipation and dynamic power reduction factor respectively. **Table 3** shows standby subthreshold leakage power dissipation and standby subthreshold leakage reduction factor for a one-bit full adder circuit, when both the proposed and existing circuit techniques are implemented in SOI CMOS technology. **Table 4** shows dynamic power dissipation and dynamic power dissipation reduction factor for a one-bit full adder circuit when both the proposed technique and existing circuit techniques are implemented in SOI CMOS technology.

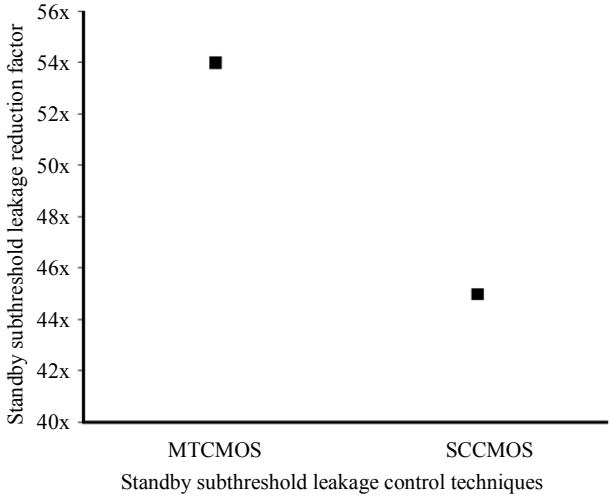

Figure 6. Standby subthreshold leakage reduction factor of the proposed technique in comparison to MTCMOS and SCCMOS techniques for a one-bit full adder circuit.

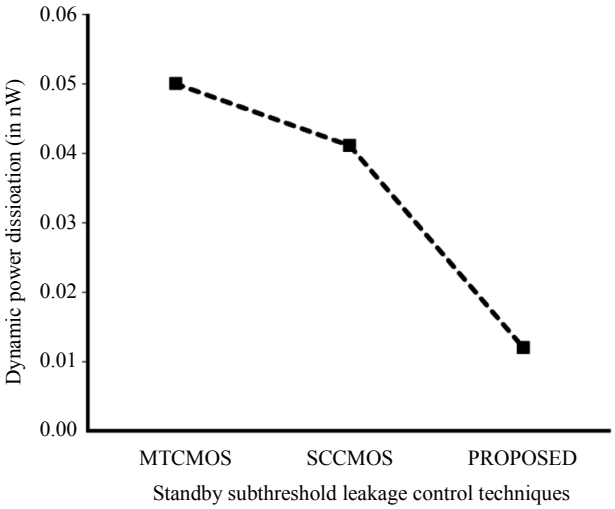

Figure 7. Dynamic power dissipation for a one-bit full adder circuit in MTCMOS, SCCMOS and proposed techniques.

Table 3. Standby subthreshold leakage power dissipation and standby subthreshold leakage reduction factor for a one-bit full adder circuit when both the existing techniques and the proposed technique are implemented in SOI CMOS technology.

Techniques	Dynamic power dissipation	Dynamic power dissipation reduction factor for the proposed technique in comparison with existing techniques
Multi-Threshold	0.037 µW	3.083x
Super Cutoff	0.031 µW	2.583x
Proposed	0.012 µW	-

Reduction in the standby subthreshold leakage power dissipation by reduction factors of 54x and 45x foraone-bit full adder circuit is achieved using the proposed SOI CMOS based circuit technique in comparison to the existing MTCMOS and SCCMOS techniques respectively in CMOS bulk technology. Dynamic power dissipation is also reduced significantly by reduction factors of 4.167x and 3.417x using the proposed SOI CMOS technology based circuit technique in comparison with MTCMOS and SCCMOS techniques respectively in CMOS bulk technology. It is also observed from **Tables 3** and **4** that the standby subthreshold leakage power dissipation and dynamic power dissipation are also reduced significantly using the proposed circuit technique in comparison with other existing techniques, when all circuit techniques are implemented in SOI CMOS technology.

Table 4. Dynamic power dissipation and dynamic power reduction factor for a one-bit full adder circuit using both the existing techniques and the proposed technique in SOI CMOS technology.

Standby subthreshold leakage reduction factor using the proposed technique in SOI CMOS technology in comparison with existing techniques in CMOS bulk technology		Dynamic power dissipation reduction factor using the proposed technique in SOI CMOS technology in comparison with existing techniques in CMOS bulk technology	
MTCMOS technique	SCCMOS technique	MTCMOS technique	SCCMOS technique
54x	45x	4.167x	3.417x

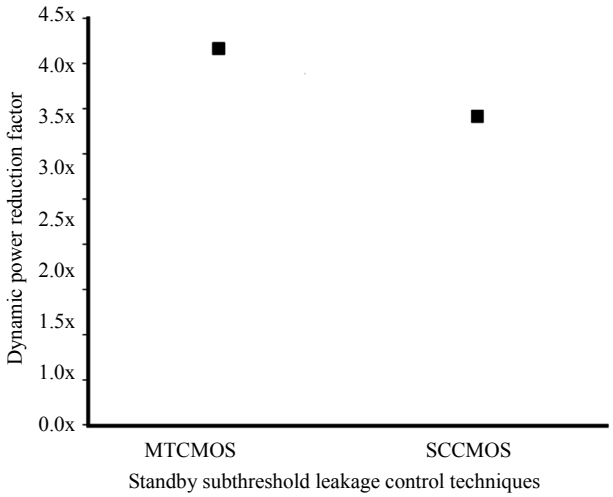

Figure 8. Dynamic power reduction factor of the proposed technique in comparison to MTCMOS and SCCMOS techniques for a one-bit full adder circuit.

7. Conclusion

This paper has presented migration of standby subthreshold leakage control technique from a bulk CMOS to SOI CMOS technology. An improved SOI CMOS technology based circuit technique for efficient reduction

of standby subthreshold leakage power dissipation is presented in this paper. The proposed technique is validated through layout design and simulation of a one-bit full adder circuit using the proposed and other existing standby subthreshold leakage control techniques. The proposed SOI CMOS technology based circuit technique dissipated the least standby subthreshold leakage power in comparison to other existing techniques in CMOS bulk technology. Dynamic power dissipation is also reduced using this proposed technique in SOI technology in comparison with other presented techniques in CMOS bulk technology. It also reveals that when both the proposed and existing techniques are implemented in SOI CMOS technology, the proposed technique maintains the trend of reduced power dissipation in both standby and dynamic modes. Hence it may be concluded that the proposed SOI CMOS technology based circuit technique showed a significant improvement in the standby subthreshold leakage power dissipation, which makes it attractive for ultra low-power applications.

8. Acknowledgements

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