Electronically-Controllable Grounded-Capacitor-Based Grounded and Floating Inductance Simulated Circuits Using VD-DIBAs

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ABSTRACT

New Voltage Differencing Differential Input Buffered Amplifier (VD-DIBA) based lossless grounded and floating inductance simulation circuits have been proposed. The proposed grounded simulated inductance circuit employs a single VD-DIBA, one floating resistance and one grounded capacitor. The floating simulated inductance (FI) circuits employ two VD-DIBAs with two passive components (one floating resistance and one grounded capacitor). The circuit for grounded inductance does not require any realization conditions whereas in case of floating inductance circuits, a single matching condition is needed. Simulation results demonstrating the applications of the new simulated inductors using CMOS VD-DIBAs have been included to confirm the workability of the new circuits.

Keywords: VD-DIBA; Inductance Simulation; Filters

1. Introduction

The importance of grounded and floating simulated inductors in the context of active network synthesis is well known [1]. Several grounded and floating inductance simulation schemes, employing different active elements such as operational amplifiers (op-amps) [2-6], current conveyors (CCs) [7-15], current controlled conveyors (CCCIIs) [16,17], current feedback operational amplifiers (CFOAs) [18,19], operational mirrored amplifiers (OMAs) [20], differential voltage current conveyors (DVCCIs) [21], current differencing buffered amplifiers (CDBAs) [22,23], current differencing transconductance amplifiers (CDTAs) [24,25], operational transconductance amplifiers (OTAs) [26,27] have been reported in the literature. In [28], many new active building blocks have been introduced; VD-DIBA is one of them. Till now, some applications of VD-DIBAs have been reported in the open literature such as in the realization of all pass filters [29], realization of grounded and floating inductance circuits using two/three VD-DIBAs as reported in [30], electronically controllable sinusoidal oscillator in [31] and voltage-mode universal biquad in [32,33]. The purpose of this paper is to introduce new VD-DIBA-based: 1) a lossless grounded inductor using only a single VD-DIBA, one resistor and a grounded capacitor without requiring any matching condition and 2) two floating inductance simulation circuits employing two VD-DIBAs, one resistor and a grounded capacitor along with a single matching condition for floatation. The genesis of these FI circuits is inspired by [1,34,35].

2. The Proposed New Configuration

The schematic symbol and equivalent model of the VD-DIBA (−) are shown in Figures 1(a) and (b) respectively [29]. The model of VD-DIBA (−) includes two controlled sources: the current source controlled by differential voltage \( V'_2 - V'_1 \), with the transconductance \( g_m \), and the voltage source controlled by differential voltage \( -V'_2 + V'_1 \), with the unity voltage gain. The VD-DIBA (−) can be described by the following set of equations:
The proposed grounded and floating inductance circuits are shown in Figure 2 and Figure 3 respectively.

A routine analysis of the circuit shown in Figure 2 results in the following expression for the input impedance:

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = s\left(\frac{C_0 R_1}{g_m}\right)$$ (2)

The circuit, thus, simulates a grounded inductance with the inductance value given by

$$L_{eq} = \frac{C_0}{g_m}$$ (3)

The proposed CMOS implementation of VD-DIBA (−) is shown in Figure 4. The CMOS VD-DIBA (−) is implemented using 0.35 µm MIETEC real transistor model which are listed in Table 1. Aspect ratios of transistors used are given in Table 2.

3. Non-Ideal Analysis and Sensitivity Performance

Let $R_z$ and $C_z$ denote the parasitic resistance and parasitic capacitance of the Z-terminal. Taking into account the non-idealities of the VD-DIBA (−), namely

$$V_w = (-\beta' V_z + \beta V_1),$$

where $\beta' = 1 - \varepsilon_1 (\varepsilon_1 \ll 1)$ and $\beta' = 1 - \varepsilon_2 (\varepsilon_2 \ll 1)$ are voltage tracking errors of the VD-DIBA, for the circuit shown in Figure 2, the non-ideal input impedance is found to be

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = s\left(\frac{C_0 R_1}{g_m g_{m2}}\right)$$ (4)

which proves that the circuits simulate a floating lossless inductance with the inductance value given by

$$L_{eq} = \frac{C_0}{g_m g_{m2}}$$ (5)
Figure 4. Proposed CMOS Implementation of VD-DIBA, $V_{DD} = -V_{SS} = 2$ V, $V_{R1} = -0.44$ V, $V_{R2} = I_{R3} = -0.22$ V and $V_{R4} = -0.9$ V.

Table 1. CMOS process parameters.

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<tr>
<th>Transistor</th>
<th>N MOS</th>
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<td>LEVEL</td>
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<td>TOX</td>
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<td>MJSW</td>
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Table 2. Dimensions of CMOS transistors.

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<tr>
<td>M7-M9</td>
<td>14/0.35</td>
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<td>M10-M18</td>
<td>4/1</td>
</tr>
<tr>
<td>M19-M22</td>
<td>7/0.35</td>
</tr>
</tbody>
</table>

Figure 5. Non-ideal equivalent circuit of grounded inductor of Figure 2.

The non-ideal equivalent circuit is given by:

$$Z_{in}(s) = \frac{s(C_1 + C_z) + \frac{1}{R_t}}{s + \frac{(C_1 + C_z)(1 - \beta^-)}{R_t} + \frac{(1 - \beta^-)}{R_z} + \beta^+ g_m + \frac{1}{R_z}}$$

where

$$L = \frac{(C_1 + C_z) R_z R_{in}}{(1 - \beta^-) + \beta^+ g_m R_{in} R_z}, \quad R' = \frac{R_t}{(1 - \beta^-)}, \quad C' = \frac{(C_1 + C_z)(1 - \beta^-) R_z}{R_t}.$$
and \( R^* = \frac{R_g}{\left(1 - \beta - \beta^* g_m R_Z\right)} \)

From the above, the sensitivities of \( L \) with respect to various active and passive elements are found to be

\[
S_{g_m}^L = \frac{C_z}{(C_1 + C_z)} , S_{g_m}^L = \frac{C_z}{(C_1 + C_z)} , S_{g_m}^L = 1,
\]

\[
S_{g_m}^R = \frac{(1 - \beta^* g_m R_Z)}{(1 - \beta - \beta^* g_m R_Z)} ,
\]

\[
S_{g_m}^\beta = \frac{\beta^* g_m R_Z}{(1 - \beta - \beta^* g_m R_Z)} ,
\]

\[
S_{g_m}^\beta = -\frac{\beta^* g_m R_Z}{(1 - \beta + \beta^* g_m R_Z)} ,
\]

\[
S_{g_m}^\beta = -\frac{\beta^* g_m R_Z}{(1 - \beta + \beta^* g_m R_Z)}
\]

Similarly, for the circuit shown in Figures 3(a) and (b) for \( \beta^* = \beta^* = 1 \), the input-output currents and voltages relationships are given by:

\[
\begin{bmatrix}
I_1 \\
I_2
\end{bmatrix} = \frac{g_m g_m}{s(C_0 + C_{zi}) + \frac{1}{R_{zi}}}
\times \begin{bmatrix}
1 & -1 \\
-1 & 1 + \frac{1}{g_m g_m}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix}
\]

with \( g_m^2 = \frac{1}{R_0} \)

The non-ideal equivalent circuit of floating inductors of Figures 3(a) and (b) derivable from Equation (8) is shown in Figure 6.

Where \( L = \frac{(C_0 + C_{zi})}{g_m g_m} \) and \( R = \frac{1}{R_{zi} g_m g_m} \)

The various sensitivities of \( L \) with respect to active and passive elements are:

\[
S_{g_m}^L = \frac{C_z}{C_z} , S_{g_m}^L = \frac{C_z}{C_z} , S_{g_m}^L = 1 ,
\]

\[
S_{g_m}^R = -1 , S_{g_m}^\beta = 0 , S_{g_m}^\beta = 0
\]

Taking \( g_m = g_m = 389.673 \mu A/V , C_0 = C_{zi} = 0 , R_0 = R_{zi} = \infty , C_0 = 0.1 \text{ nF} \) and \( R_0 = 100 \text{ k} \Omega \), these sensitivities are found to be \((1, 0, 1, 0, 0, -1)\) and \((1, 0, -1, -1, 0, 0)\) for Equations (7) and (9) respectively. Thus, all the passive and active sensitivities of both grounded and floating inductance circuits are low.

4. Simulation Results of the New Proposed Grounded/Floating Inductance Configurations

The workability of the proposed simulated inductors has been verified by realizing a band pass filter (BPF) as shown in Figures 7 and 8.

The transfer function realized by this configuration is given by

\[
\frac{V_0}{V_m} = \frac{s\left(\frac{1}{R_2 C_2}\right)}{s^2 + \frac{1}{R_2 C_2} + \frac{g_m}{C_1 C_2 R_1}}
\]

from where it is seen that bandwidth and centre frequency are independently tunable, the former by \( R_2 \) and the latter by any of \( R_1, g_m \) and \( C_1 \).

The transfer function realized by configuration shown in Figure 8 is given by
\[
\frac{V_0}{V_{in}} = \frac{s \left( \frac{R g_m g_{m_2}}{C_0} \right)}{s^2 + s \left( \frac{R g_m g_{m_2}}{C_0} \right) + g_m g_{m_2} C_0 C_1} \quad \text{with} \quad g_{m_2} = \frac{1}{R_0}.
\]

(11)

In this case, bandwidth is tunable by \( R_1 \) whereas centre frequency can be tuned by \( C_1 \).

Performance of the new simulated inductors was verified by SPICE simulations. CMOS-based VD-DIBA (−) (as shown in Figure 4) was used to determine the frequency responses of the grounded and floating simulated inductors. The following values were used for grounded inductor: \( C_1 = 0.01 \text{nF}, \ R_1 = 100 \text{k}\Omega, \ g_m = 296.468 \mu\text{A/V} \) and for the floating inductor: \( C_0 = 0.01 \text{nF}, \ R_0 = 100 \text{k}\Omega, \ g_m = 296.468 \mu\text{A/V} \) and \( g_{m_2} = 10 \mu\text{A/V} \). From the frequency response of the simulated grounded inductor (Figure 9) it has been observed that the inductance value remains constant up to 1 MHz. Similarly, from the frequency response of the simulated floating inductor (Figure 10) the inductance value also remains constant up to 1 MHz.

To verify the theoretical analysis of the application circuits shown in Figures 7 and 8, they have also been simulated using CMOS-based VD-DIBA (−) as shown in Figure 4. The component values used were for Figure 7: \( C_1 = 0.1 \text{nF}, \ C_2 = 1 \text{pF}, \ R_1 = 100 \text{k}\Omega, \ R_2 = 113.258 \text{k}\Omega \) and for Figures 8(a) and (b): \( C_0 = 0.1 \text{nF}, \ C_1 = 0.01 \text{nF}, \ R_0 = 100 \text{k}\Omega, \ R_1 = 71.652 \text{k}\Omega, \ g_{m_2} = 10 \mu\text{A/V} \) (which can be maintained by taking \( V_{B1} = -1.5 \text{V} \)). The VD-DIBA was biased with ±2 volts D.C. power supplies with \( V_{B1} = -0.44 \text{V}, \ V_{B2} = V_{B3} = -0.22 \text{V} \) and \( V_{B4} = -0.9 \text{V} \). VD-DIBA (−) transconductance is controlled by \( V_{B1} \).

Figure 11, Figures 12(a) and (b) show the simulated filter responses of the BP filters.

The above described results, thus, confirm the validity of the application of the proposed grounded and floating simulated inductance circuits. A comparison of the various salient features of the proposed configurations as compared to other previously known grounded and FI......
Figure 10. Frequency response of the simulated floating inductor.

Figure 11. Frequency response of BPF using the proposed simulated grounded inductor.

Figure 12. Frequency response of BPF using the proposed simulated floating inductor.
Table 3. Comparison with other previously published grounded and floating inductors.

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<th>Number of resistors used</th>
<th>Number of capacitors used</th>
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<th>Availability of Electronic tunability</th>
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*F = Floating, G = Grounded.

Simulators has been included in Table 3.

5. Conclusions

New circuits of lossless grounded and floating inductance have been proposed employing VD-DIBAs. The proposed grounded inductance circuit employs only one VD-DIBA (−), one resistor and one grounded capacitor and does not require any component matching condition. On the other hand, the two floating inductance configurations each using two VD-DIBAs (−), one resistor and one grounded capacitor, need only a single realization condition for floatation. The SPICE simulation results have confirmed the workability of the new propositions as well as the suggested application examples using them.

The problem of realizing any new single VD-DIBA-based FI configuration using a single grounded capacitor and without requiring any matching condition appears to be an interesting problem which is open to be investigated.

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