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New Hybrid Digital Circuit Design Techniques for Reducing Subthreshold Leakage Power in Standby Mode

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ABSTRACT

In this paper, four new hybrid digital circuit design techniques, namely, hybrid multi-threshold CMOS complete stack technique, hybrid multi-threshold CMOS partial stack technique, hybrid super cutoff complete stack technique and hybrid super cutoff partial stack technique, have been proposed to reduce the subthreshold leakage power dissipation in standby modes. Techniques available in literature are compared with our proposed hybrid circuit design techniques. Performance parameters such as subthreshold leakage power dissipation in active and standby modes, dynamic power dissipation and propagation delay, are compared using existing and proposed hybrid techniques for a two input AND gate. Reduction of subthreshold leakage power dissipation in standby mode is given more importance, in comparison with the other circuit design performance parameters. It is found that there is reduction in subthreshold leakage power dissipation in standby and active modes by 3.5× and 1.15× respectively using the proposed hybrid super cutoff complete stack technique as compared to the existing multi-threshold CMOS (MTCMOS) technique. Also a saving of 2.50× and 1.04× in subthreshold leakage power dissipation in standby and active modes respectively were observed using hybrid super cutoff complete stack technique as compared to the existing super cutoff CMOS (SCCMOS) technique. The proposed hybrid super cutoff stack technique proved to perform better in terms of subthreshold leakage power dissipation in standby mode in comparison with other techniques. Simulation results using Microwind EDA tool in 65 nm CMOS technology is provided in this paper.

1. Introduction

Design of low power circuit is necessary for portable electronic devices that are powered by batteries as increased power dissipation reduces the battery lifetime. Low power dissipation by MOS transistors and its small size for greater integration capacity are the major factors behind shifting in technology from BJTs to MOSFETs. High power dissipation is one of the major challenges of integrated circuit design in deep submicron and nanoscale technologies [1-5]. The demand for higher functions with higher performance and lower power dissipation initiates the scaling of MOS transistors in every technology generations. The contribution of dynamic power in the overall power dissipation decreases with the scaling of MOS transistors. Leakage power is expected to increase 32 times per device by the year 2020 [6]. Reduction of the supply voltage, V_{DD} is considered as the most effective method to reduce the dynamic power, which is directly proportional to the square of the supply voltage, V_{DD}. In order to maintain the same performance, threshold voltage of the transistor is also reduced with

the scaling of the supply voltage. However, subthreshold leakage current increases exponentially with the reduction of the threshold voltage of the MOS transistor, making it critical for low voltage digital integrated circuit design. Scaling of transistors in every technology generations also lead to increase in the subthreshold leakage current. With rapid scaling in technology, the increase in leakage current has made leakage power a significant part in the overall power dissipation in both active and standby modes. The major components of leakage power dissipation are subthreshold leakage, gate leakage, gate induced drain leakage, and forward biased diode leakage [7]. Subthreshold leakage dominates the other leakage components in deep submicron and nanoscale technologies.

Threshold voltage of transistors used in design of digital circuits should be adjusted for maximum saving in the leakage power dissipation. Circuit techniques play a very important role to control the subthreshold leakage power dissipation in both active and standby modes. Already some techniques, such as Multi-threshold CMOS

(MTCMOS) technique [8,9], Super cutoff CMOS technique [10], Stack technique [11-13] and Sleepy stack technique [14] are available in literature to control the subthreshold leakage power dissipation in deep submitcron and nanoscale technologies. Each technique has its own advantages and disadvantages. Depending upon the requirement and application, chip designers can choose the appropriate circuit design technique.

In this paper, four new digital circuit design techniques namely, hybrid multi-threshold CMOS complete stack technique, hybrid multi-threshold CMOS partial stack technique, hybrid super cutoff complete stack technique and hybrid super cutoff partial stack technique are presented. These techniques are applied to a two input AND gate to evaluate their performance. It is found that the proposed techniques give improved performance in terms of reduced subthreshold leakage power dissipation in standby mode as compared with the other techniques available in the literature [8-14].

2. Subthreshold Leakage Power Dissipation

Subthreshold or weak inversion conduction current is the current flow between source and drain region in a MOS transistor, even when gate voltage, V_{GS} is below the threshold voltage, V_{TH} of the MOS transistor. It is due to the minority carrier drift through the channel from the drain to the source region in weak inversion region. **Figure 1** shows the flow of subthreshold leakage current in an nMOS transistor, when V_{GS} is less than V_{TH} of the transistor. **Figure 2** [15] shows the variation of minority carrier concentration along the length of the channel for an n-channel MOSFET biased in the weak inversion region. This figure shows that the concentration of minority carriers in weak inversion region is small, but not zero. Subthreshold leakage power dominates the other leakage power components because of the necessity to use low threshold voltage transistors to maintain the desired performance of the device. This leakage power should be minimized through new and improved circuit design techniques. This leakage power dissipation is undesirable in digital circuit design.

According to BSIM4 MOSFET model, the equation governing this subthreshold leakage current can be expressed as [16]

$$I_{SUB} = I_0 e^{\frac{V_{GS}-V_{THO}-\eta V_{DS}+\gamma V_{BS}}{nV_T}}\left(1-e^{\frac{-V_{DS}}{V_T}}\right) \quad (1)$$

where,

$$I_0 = \mu C_{ox}\left(\frac{W}{L}\right)V_T^2 e^{1.8} \text{ and } V_T = \frac{KT}{q} \quad (2)$$

Here V_{GS}, V_{DS} and V_{BS} are the gate to source, drain to source, and bulk to source voltages respectively, μ denotes the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W and L denote the channel width and channel length of the transistor, K is the Boltzmann constant, T is the absolute temperature, q is the electrical charge of an electron, V_T is the thermal voltage, V_{TH0} is the zero biased threshold voltage, γ is body effect coefficient, η denotes the drain induced barrier lowering coefficient, and n is the subthreshold swing coefficient. Equation (1) reveals that the subthreshold leakage current is a strong function of the threshold voltage and the voltages of all the four terminals of the MOS transistor.

The Berlkeley Short-Channel IGFET model [17] is used for the calculation of the threshold voltage of a MOS transistor and is expressed as:

$$V_{TH} = V_{FB} + \varphi_s + K_1\left(\varphi_s\right)^{1/2} - K_2\varphi_s - \eta V_{DD} \quad (3)$$

where V_{FB} is the flatband voltage, φ_s is two times the Fermi potential, K_1, and K_2 terms represent the non-uniform doping effect, and η denotes the drain induced barrier lowering coefficient.

3. Circuit Design Methodology Adopted for Reducing Subthreshold Leakage Power in Standby Mode

Subthreshold leakage power reduction in standby mode is significant in burst mode type circuits, where compu-
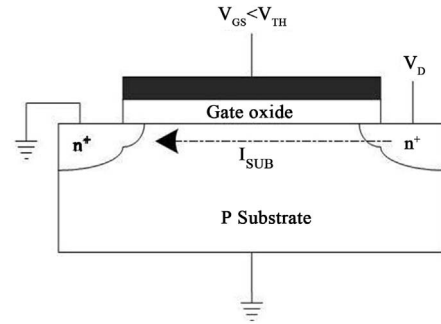

Figure 1. Subthreshold leakage current in an nMOS transistor.
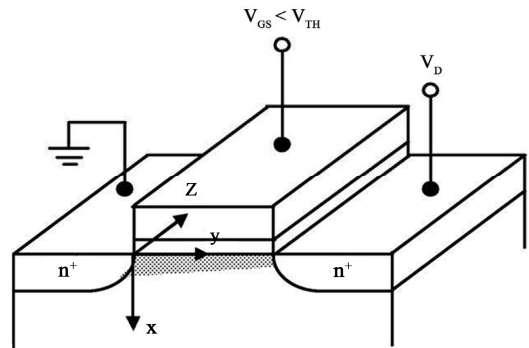

Figure 2. Variation of minority carrier concentration in an nMOS transistor in weak inversion.

tation occurs only during short burst intervals, and the system is in standby mode for the majority of the time [18]. The wastage of useful battery power during long standby period is highly undesirable. New circuit techniques must be devised to control the subthreshold leakage power dissipation in standby mode for burst mode applications. Portable battery operated devices that remain in standby mode for most of the times are greatly affected by standby subthreshold leakage power loss. Existing circuit design techniques must therefore be modified in such a way that it curbs the draining of battery current when it is not operational. **Table 1** [19] shows the dependence of subthreshold leakage current on MOS device parameters. Increasing the threshold voltage of the MOS transistor is an effective way to reduce subthreshold leakage power dissipation.

Stack effect or Self-Reverse bias effect is the phenomenon where subthreshold leakage current decreases due to two or more series connected turned off transistors. Stacking of transistor is done by replacing transistor of width W with two series connected transistors of width W/2. **Figure 3** shows the natural stacking of nMOS transistors in a two input NAND gate. When both nMOS transistors Q_1 and Q_2 are turned off, then the intermediate node voltage, V_Q raises to a positive value due to the presence of a small drain current.

Table 1. Dependence of subthreshold leakage current on MOS transistor parameters.

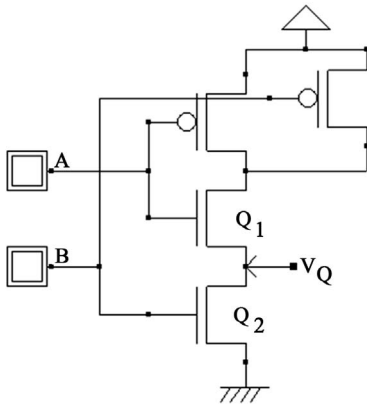| Transistor parameter	Dependence of subthreshold leakage
Transistor width (W)	Directly proportional
Transistor length (L)	Inversely proportional
Temperature (T)	Exponential increase
Transistor threshold voltage (V_{TH})	Increases by an order of magnitude with 100 mV decrease
Input voltage (V_{GS})	Exponential increase

Figure 3. Natural stacking of nMOS transistors in a two input NAND gate.

Positive potential $\left(V_Q > 0\text{V}\right)$ at the intermediate node between two turned off stacked transistors has following effects [19,20]:

1) V_{GS} of Q_1 becomes negative;

2) V_{BS} of Q_1 becomes negative, causing an increase in V_{TH} of Q_1 due to an increase in the body effect of Q_1;

3) V_{DS} of Q_1 decreases, resulting in less drain induced barrier lowering.

From Equation (1), it is observed that a negative V_{GS}, an increase in the body effect (negative V_{BS}), and a reduction in V_{DS} (less drain induced barrier lowering) reduce the subthreshold leakage current exponentially in standby mode.

4. Proposed Hybrid Circuit Techniques

In this section, we propose four new digital circuit techniques namely, hybrid MTCMOS complete stack technique, hybrid MTCMOS partial stack technique, hybrid super cutoff complete stack technique and hybrid super cutoff partial stack technique, for the reduction of subthreshold leakage power dissipation in standby modes. First two techniques are grouped as hybrid MTCMOS stack technique and last two techniques as hybrid super cutoff stack technique. Proposed techniques are discussed as follows.

4.1. Hybrid Multi-Threshold CMOS Stack Technique

This technique combines the advantages of both MTCMOS and Stack techniques. This proposed hybrid technique is further classified, as given above, into two types depending on the stacking of transistors.

4.1.1. Hybrid Multi-Threshold CMOS Complete Stack Technique

The proposed logic circuit for hybrid MTCMOS complete stack technique is shown in **Figure 4**. In this technique, a high threshold voltage pMOS transistor (sleep pMOS transistor) is inserted between V_{DD} and the pull up network and a high threshold voltage nMOS transistor (sleep nMOS transistor) is inserted between the pull down network and GND. Then stacking of all transistors (high V_{TH} sleep pMOS, high V_{TH} sleep nMOS and low V_{TH} transistors of the logic circuit) are done by replacing each transistor of width W with two series connected transistors of width W/2. During standby mode, the sleep signal is active high, making the stacked sleep transistors in cutoff state. So, the logic circuit is disconnected from V_{DD} and GND. This reduces the subthreshold leakage power dissipation significantly by utilizing stacking effect in both high V_{TH} sleep nMOS and sleep pMOS transistors during their cutoff states. The high V_{TH} nMOS and pMOS stacked sleep transistors are turned on during

normal or active circuit operation, when the sleep signal is active low.

4.1.2. Hybrid MTCMOS Partial Stack Technique

The proposed logic circuit for hybrid MTCMOS partial stack technique is shown in **Figure 5**. In this technique, a high V_{TH} pMOS transistor (sleep pMOS transistor) is inserted between V_{DD} and the pull up network and a high V_{TH} nMOS transistor (sleep nMOS transistor) is inserted between the pull down network and GND. Then stacking of only high V_{TH} sleep pMOS and high V_{TH} sleep nMOS transistors are done. In this technique, stacking of low V_{TH} nMOS and pMOS transistors of the logic circuit is not performed. Here, only partial stacking of high V_{TH} sleep pMOS and sleep nMOS transistors are done to reduce the overall circuit propagation delay in active mode. During standby mode (when sleep signal is active high), the stacked high V_{TH} sleep pMOS and sleep nMOS transistors are turned off, thereby, reducing significant subthreshold leakage power dissipation. In active mode, the stacked sleep transistors are turned on. The circuit propagation delay using this technique in active mode is slightly reduced as compared to the previous technique because of partial stacking of transistors (stacking of only sleep pMOS and sleep nMOS transistors).
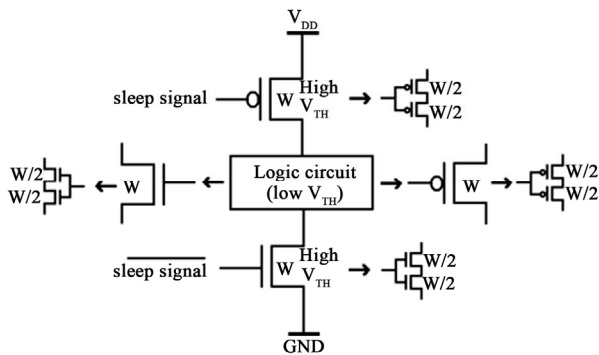

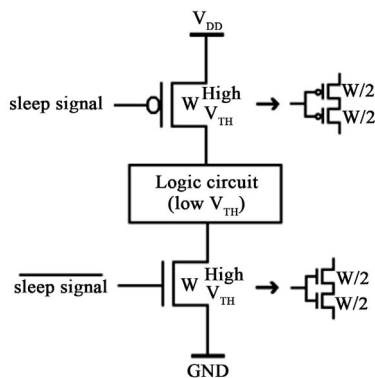**Figure 4. Logic circuit using hybrid MTCMOS complete stack technique.**

Figure 5. Logic circuit using hybrid MTCMOS partial stack technique.

4.2. Hybrid Super Cutoff Stack Technique

This hybrid technique combines the advantages of both Super cutoff CMOS (SCCMOS) and Stack techniques. The proposed hybrid technique can further be classified into two types, namely hybrid super cutoff complete stack technique and hybrid super cutoff partial stack technique, depending on the stacking of transistors.

4.2.1. Hybrid Super Cutoff Complete Stack Technique

This technique is similar to hybrid MTCMOS complete stack technique. The only difference lies in the use of low V_{TH} sleep pMOS and low V_{TH} sleep nMOS transistors. **Figure 6** shows the logic circuit using this hybrid technique. In this technique, positive and negative gate voltages are used to completely turnoff sleep pMOS and sleep nMOS transistors respectively in standby mode. During standby state (when sleep signal is active high), the subthreshold leakage power dissipation reduces exponentially because of the use of negative and positive gate voltages to nMOS and pMOS sleep transistors respectively and also due to the stacking effect in series connected cutoff stacked sleep transistors. In active mode, these sleep transistors having low V_{TH} are turned on and thus provide low resistance input-output path. In active mode, the circuit propagation delay using this technique is reduced as compared to the hybrid multi-threshold CMOS stack technique because of the use of low V_{TH} sleep transistors.

4.2.2. Hybrid Super Cutoff Partial Stack Technique

This hybrid technique is similar to hybrid MTCMOS partial stack technique. The difference lies in the use of low V_{TH} sleep nMOS and pMOS transistors. **Figure 7** shows the logic circuit using this technique. During standby mode, the subthreshold leakage power dissipation reduces exponentially because of use of negative and positive gate voltages to nMOS and pMOS sleep transistors respectively and also due to stacking effect in series connected cutoff stacked sleep transistors. The major
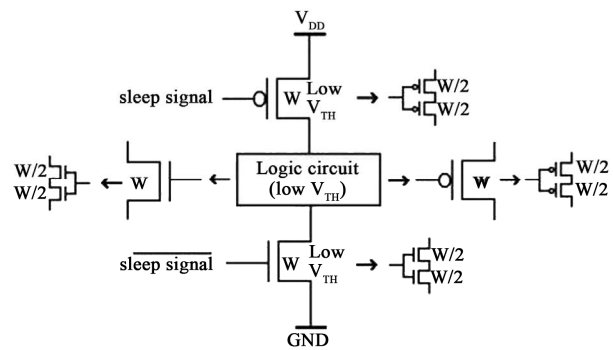

Figure 6. Logic circuit using hybrid super cutoff complete stack technique.

advantage in using this technique is further reduction in the overall circuit propagation delay in active mode as compared with the hybrid super cutoff complete stack technique because of the use of only partial stacking of sleep pMOS and sleep nMOS transistors.

5. Result and Discussion

To compare the performance, the proposed techniques are applied to a two input AND gate. The performance parameters such as subthreshold leakage power dissipation in active and standby modes, dynamic power dissipation and propagation delay of a two input AND gate were analysed in 65 nm technology using existing [10-16] and proposed hybrid techniques. Layouts of a two input logic AND gate using various techniques were simulated using Microwind EDA tool at a temperature of 27°C and V_{DD} of 0.7 V. The threshold voltage of high V_{TH} transistor was taken as two times of V_{TH} of normal transistor of the logic circuit. The threshold voltage of normal nMOS and pMOS transistors (low V_{TH}) were taken as 0.20 V and −0.20 V respectively. **Figures 8** and **9** show the
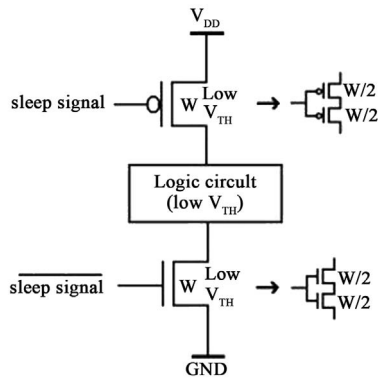
Figure 7. Logic circuit using hybrid super cutoff partial stack technique.

simulated layout diagrams of a two input AND gate using hybrid super cutoff complete stack and hybrid super cutoff partial stack techniques respectively. **Figure 10** shows the output waveform of a two input AND gate in presence of a sleep signal.

Subthreshold leakage power dissipation was measured by combining all possible input vectors. The voltage magnitude of input vector should always be less than the threshold voltage of the normal transistor of the logic circuit. Sleep nMOS and sleep pMOS transistors were turned off during measurement of subthreshold leakage power dissipation in standby mode while for its measurement in active mode, all sleep nMOS and sleep pMOS transistors were turned on. Subthreshold leakage power dissipation in active and standby modes for a two input AND gate for each input combination were measured for 50 ns time interval.

Dynamic power dissipation was measured by applying input pulse signals of same frequency with a fixed delay between them. Two input pulse signals of V_{DD} of 0.7 V and frequency of 250 MHz were applied to a two input AND gate. All sleep nMOS and sleep pMOS transistors were turned on during measurement of dynamic power dissipation. The dynamic power dissipation was measured for a two input AND gate for 50 ns time interval.

Propagation delay of the logic circuit was measured from the trigger input edge reaching 50% of V_{DD} to the circuit output edge reaching 50% of V_{DD}.

Table 2 shows various performance parameters measurement of a two input AND gate using existing [8-14] and proposed hybrid techniques.

Subthreshold leakage power dissipation in active and standby modes of a two input AND gate are compared using existing [10-16] and proposed techniques in **Figure 11**. Subthreshold leakage power dissipation of a two input AND gate in standby mode in 65 nm technology is
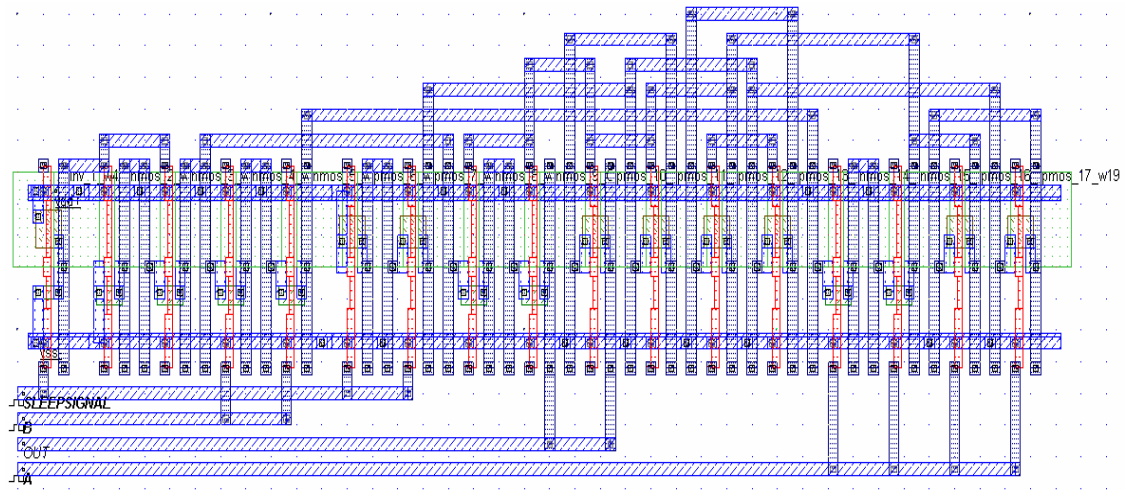
Figure 8. Layout of a two input AND gate using hybrid super cutoff complete stack technique.
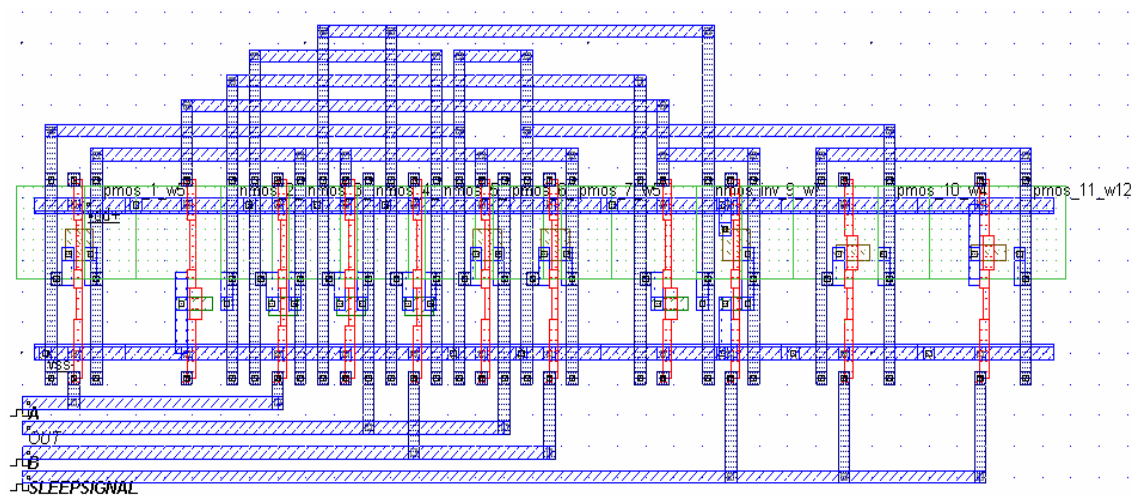
Figure 9. Layout of a two input AND gate using hybrid super cutoff partial stack technique.
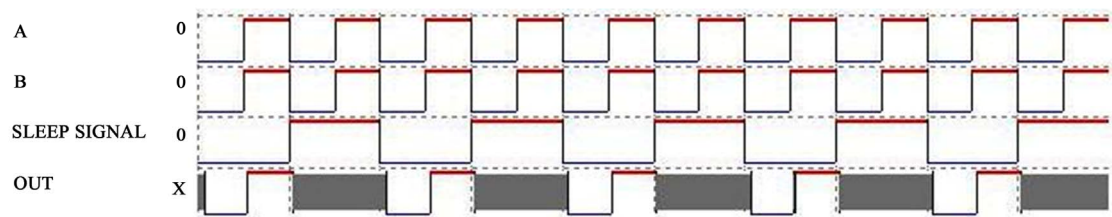

Figure 10. Output waveform of a two input AND gate in presence of a sleep signal.

Table 2. Performance parameter measurements of a two input AND gate.

Reference	Technique	Subthreshold leakage power (in nW)		Dynamic power (in µW)	Propagation delay (in sec.)
		Active mode	Standby mode		
[8-9]	MTCMOS	186.00	7.00	0.87	14.2×10^{-12}
[10]	Super cutoff CMOS	168.00	5.00	0.78	21.2×10^{-13}
[11-13]	Stack	110.00	18.00	0.98	22.1×10^{-12}
[14]	Sleepy stack	172.00	19.00	1.12	18.7×10^{-12}
Proposed	Hybrid MTCMOS complete stack	169.00	03.00	1.68	32.1×10^{-12}
Proposed	Hybrid MTCMOS partial stack	157.00	03.40	1.45	19.1×10^{-12}
Proposed	Hybrid Super cutoff complete stack	161.00	02.00	1.52	41.2×10^{-13}
Proposed	Hybrid super cutoff partial stack	147.00	02.45	1.36	31.8×10^{-13}

better using the proposed hybrid super cutoff technique. The proposed hybrid super cutoff stack technique proved to perform better in terms of subthreshold leakage power dissipation in standby mode in comparison with other techniques. Results show that the subthreshold leakage power dissipation in standby and active modes are reduced by 3.5× and 1.15× using the proposed hybrid super cutoff complete stack technique as compared to the existing multi-threshold CMOS (MTCMOS) technique. Also a saving of 2.5× and 1.04× in subthreshold leakage power dissipation in standby and active modes

are observed using hybrid super cutoff complete stack technique as compared to the existing super cutoff CMOS (SCCMOS) technique. It is also observed that the propagation delay reduces sharply in comparison to MTCMOS technique; however dynamic power dissipation increases slightly vis-à-vis super cutoff CMOS technique. Although dynamic power dissipation is slightly higher, the proposed technique is very much effective for the applications, specially, where the reduction of subthreshold leakage power dissipation in standby mode is warranted for.
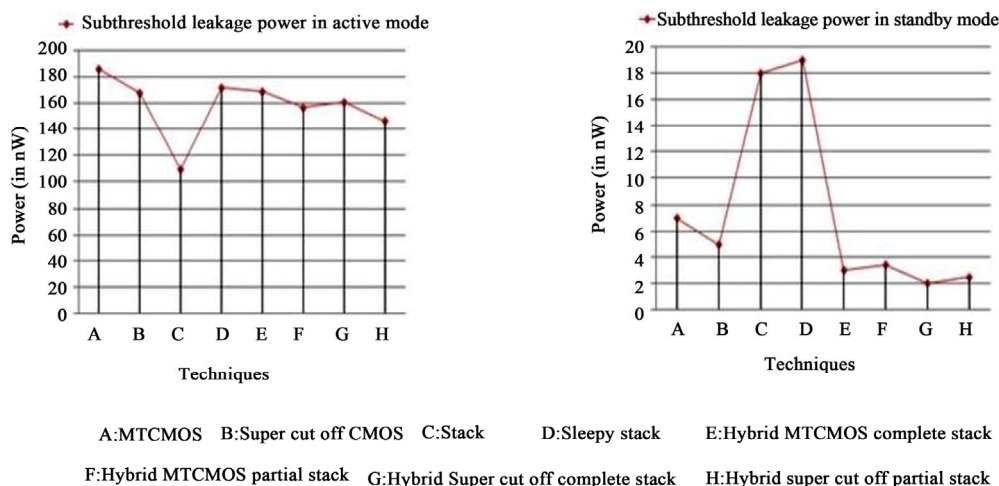
Figure 11. Subthreshold leakage power in active and standby modes.

6. Conclusion

Subthreshold leakage power reduction in standby mode is very much essential for burst mode type circuits, where computation occurs only during short burst intervals, and the system is in standby mode for the majority of the time. The wastage of useful battery power during long standby period is highly undesirable. Portable electronic appliances such as cell phones and pagers are used in active mode for a very short time interval. These appliances drain their useful battery power for a very long standby period. Similarly, the leakage of battery power in portable laptop during standby mode is highly undesirable. Subthreshold leakage reduction techniques during the standby mode can significantly reduce the leakage in burst mode applications. The proposed hybrid super cutoff stack technique proved to perform better in terms of subthreshold leakage power dissipation in standby mode in comparison with other techniques. It is found that there is reduction in subthreshold leakage power dissipation in standby and active modes by 3.5× and 1.15× respectively using the proposed hybrid super cutoff complete stack technique as compared to the existing multithreshold CMOS (MTCMOS) technique. Also a saving of 2.50× and 1.04× in subthreshold leakage power dissipation in standby and active modes respectively were observed using hybrid super cutoff complete stack technique as compared to the existing super cutoff CMOS (SCCMOS) technique for a two input AND gate in 65 nm technology. The proposed hybrid super cutoff stack technique proved to perform better in terms of lower subthreshold leakage power dissipation in standby mode in comparison with other existing techniques.

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