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Scientific Research

Electrical Properties of the Al/$CuInSe_2$ Thin Film Schottky Junction

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Abstract

The Schottky diode (Al/p-$CuInSe_2$/FTO) was fabricated by simple deposition of pure Aluminum on the front side of the $CuInSe_2$ thin film. We have investigated its electrical characteristics by measuring the current-voltage (I-V), the capacitance-voltage (C-V) and the electrical impedance in the range of temperature (300 K - 425 K). At room temperature, this heterostructure has shown non-ideal Schottky behavior with 3.98 as ideality factor and 38 μA/cm² as a reverse saturated current density. The C-V measured at 100 kHz has shown non-linear behavior and an increase with temperature. Similarly, we have estimated, at room temperature, the carrier doping density, the built-in potential and the depletion layer width which are of about 8.66×10^{15} cm^{-3}, 1.12 V and 0.37 μm respectively. By the impedance spectroscopy technique, we have found a decrease with temperature of all the serial resistance R_s, the parallel resistance R_p and the capacitance C_p. The frequency dependence of the imaginary part of this impedance was carried out to characterize the carrier transport properties in the heterostructure. From the Arrhenius diagram, we have estimated the activation energy at 460 meV. An equivalent electrical circuit was used for modeling these results.

Keywords

Schottky Junction, $CuInSe_2$ Thin Films, IV and CV Characteristics, Impedance Spectroscopy, Temperature Effects

1. Introduction

Photovoltaic (PV) effect was discovered in 1839, but it remained a laboratory curiosity until the mid 1950s when USA space program attempted to power satellites with PV cells. In 1954, single crystal silicon (sc-Si) PV cells of

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6% efficiency were reported at Bell Laboratories [1]. During the energy crisis of the early 1970s, both public and private sectors became interested in applications of PV energy generation. Initial efforts focused on lowering the cost of sc-Si solar cell modules since the basic technology already was well developed [2] [3], While polycrystalline silicon (pc-Si) solar cell module technology was introduced to further lower manufacturing costs. However, its cost advantages were confronted by its lower efficiency which was approximately equal to 9.2% [4]. To respond to the potential demand in the power generation market, research and development efforts were shifted gradually to other polycrystalline thin film material systems like ternary chalcopyrite semiconductors ($CuInSe_2$, $CuGaSe_2$, $AgInSe_2$, etc.) which gave efficiency from 6% to 16% [5]-[9]. These materials systems are being considered seriously as the basis of PV module future technologies for terrestrial power generation. On the other hand, several techniques have been actually used for the preparation of chalcopyrite films. We can mention some of them as electrodeposition [10] [11], flash evaporation [12], r.f. sputtering [13], thermal evaporation [14], solution growth [15], hot press [16], hot wall method [17] [18] and pulse laser ablation [19] and so on.

Although metal-semiconductor (MS) contacts are the most used as rectifying contacts for the fabrication of electronic devices, they are frequently used in solar cells, in light detectors and in integrated circuits [20]-[26]. The performance and the reliability of a Schottky diode are considerably influenced by the quality of the interface between the deposited metal and the contact surface of the semiconductor [27]. The most important physical parameters characterizing this junction are its potential barrier and its ideality factor. The existence of native oxide layer in its interface has a direct effect on the carrier charges transport and modifying the electrical properties [28]. The Schottky junction Al/$CuInSe_2$ is one of the simplest MS contact devices. The p-type junctions, like p-$CuInSe_2$, have been analyzed and have given useful information concerning the effects of the physical defects on the electrical carrier transport through the junctions [29] [30]. As proved experimentally, most of these junctions have an electrical behavior close to the theoretical ideal thermionic emission current model usually used [31]-[36], although the study of the temperature dependence on the current-voltage (IV) and the capacitance-voltage (CV) characteristics of these junctions gives more detailed information about their conduction processes and the nature of the potential barrier [37]-[43].

In this work, we have fabricated the Schottky junction Al/p-$CuInSe_2$ by electrodeposition technique to investigate the dominant current transport conduction mechanisms. The temperature dependence of the current-voltage, capacitance-voltage characteristics and the impedance measurements were analyzed in order to understand the effects of interface and the thermionic emission mechanism on this Schottky junction.

2. Experimental Details

The CIS ($CuInSe_2$) films have been electrodeposited on FTO substrates and treated at 400˚C in vacuum during 20 min as described in our previous works [10]. In order to form the Al/p-CIS/FTO Schottky junction, aluminum electrodes were evaporated on this structure as shown in **Figure 1**, following by an annealing in air at different temperature varying in the range 50˚C - 125˚C.

Their electrical properties were tested by using the AC/DC Keithley Instrument Model 4200-SCS Semiconductor Characterization System by measuring their I-V, C-V and their electrical impedances which were performed with a sweep of voltage.

3. Results and Discussion

3.1. Current-Voltage Characteristics

Schottky barriers on semiconductor are of interest not only because of their applications as rectifying contacts but also due to the insight they afford into the nature of bounding and defect levels in solids. Generally, it is assumed that the forward bias current of the Schottky diodes is due to thermionic emission mechanism.

The theoretical current–voltage characteristic of the *p–n* junction diode is given by the following known relationship [44]:

$$I = I_0\left[\exp\left(\frac{q}{nKT}\left(V - R_s I\right)\right) - 1\right] \quad (1)$$

where q is the carrier unit charge, I_0 is the reverse saturation current, V the applied voltage, R_s the serial

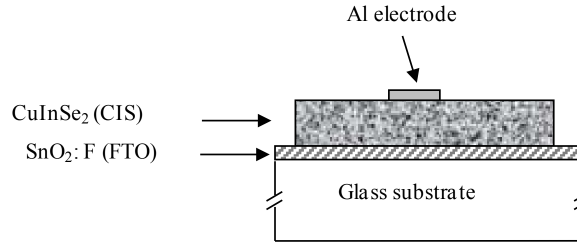

Figure 1. The structure of Al/p-CIS/FTO Schottky junction.

resistance, T the absolute temperature and n the ideality factor.

Experimentally, the current-voltage characteristic studied under forward and reverse bias conditions of the Al/p-CIS/FTO junction in dark and at room temperature is shown in **Figure 2**. The rectifying behavior confirms that this junction acts like a Shottky diode.

The approximated Equation (1) up to the threshold potential can be written in the following logarithmic form:

$$\ln I = \ln I_0 + \frac{q}{nKT}\left(V - R_s I\right) \tag{2}$$

Figure 3 shows, at room temperature, the I-V characteristic which shows the reverse current saturation about 38 μA.

Moreover, the differentiation of the last equation may provide the following form:

$$\frac{\mathrm{d}V}{\mathrm{d}\left(\ln I\right)} = R_s I + \frac{nKT}{q}$$

Figure 4 illustrates, at room temperature, this variation versus the current density *I*. It has, in fact, a linear behavior and we can easily extract both the serial resistance R_s and the ideality factor n which are estimated to be 137.5 Ω and 3.98 respectively. This last one has high value than the ideal factor $(n = 1)$ which is possibly due to the potential drop and the recombination current traversing the interfacial layer [37].

3.2. Capacitance-Voltage Measurements

The depletion layer capacitance C per unit area can be given by the known expression:

$$\mathrm{C}^{-2} = \frac{2}{q\varepsilon_s N_A}\left[V_0 - V\right] \tag{3}$$

where, ε_s is the dielectric constant of semiconductor, V the applied voltage, N_A the carrier acceptors concentration and V_0 is the built-in potential in semiconductor devices which is equal to the potential across the depletion region in thermal equilibrium.

In dark, the capacitance-voltage C^{-2}-V in the reverse bias voltage, at different temperatures and at 100 kHz, was studied. It is clear from **Figure 5** that at reverse bias ($V \le -3$ Volts) the capacitance is bias dependent which indicates that the junction is fully depleted. As the bias increases, a locally linear behavior is obtained for all temperatures.

According to Equation (3), we have extracted from **Figure 6** the built-in potential V_0 and the carrier acceptors concentration N_A at different temperatures for Al/p-$CuInSe_2$ Schottky junction. We can see that the V_0 decrease when the temperature increases and lies between 1.12 and 0.21 V and these results are comparable with other works in literatures [28] [45] [46]. While, the carrier doping density N_A value is slightly increased with temperature and varied from 8.66×10^{15} cm^{-3} at 300 K to 1.57×10^{16} cm^{-3} at 425 K. We note that the effective carrier concentration in this thin Schottky film is in order of 10^{15} cm^{-3}. These results are also in good agreement with those reported by Zhang *et al.* and other authors [47]-[49].

Thus, the annealing of the junction modifies the electrical properties in the layers. This can be attributed to the presence of the interfacial thin native oxide layer between the metal and semiconductor [50] or by the inter-diffusion between the metal layer and the CIS film and may be also due to the existence of a trap centers in the junction [51] [52].

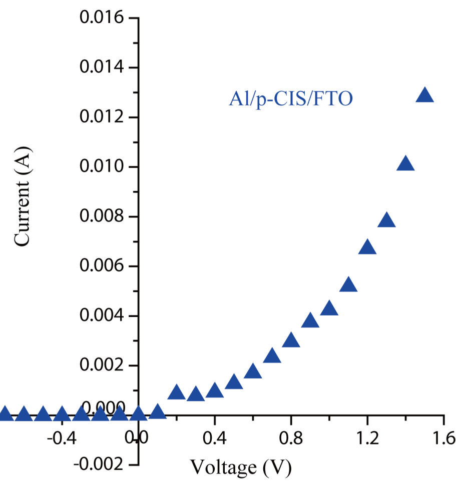

Figure 2. Experimental current-voltage characteristic of Al/p-CIS junction at room temperature.

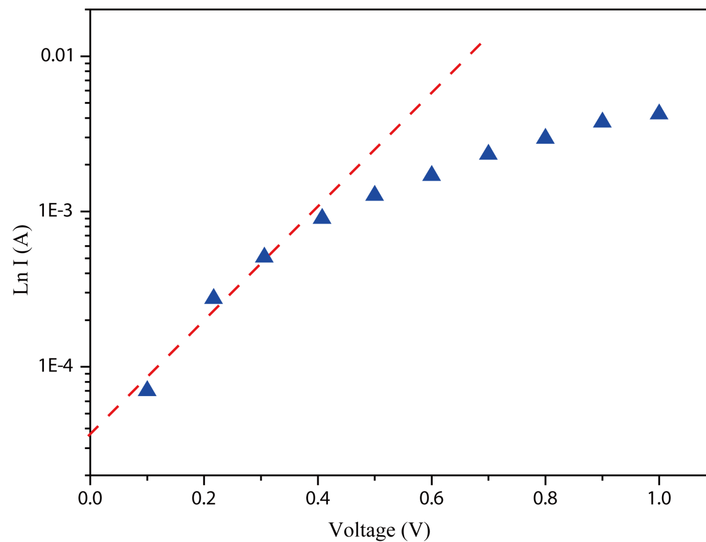

Figure 3. The logarithm of the current density ln(*I*) vs. the forward bias voltage (*V*) of The Al/p-CIS Schottky junction at room temperature.

In addition, the defects in semiconductor material play an important role as traps or as recombination centers depending on the capture cross section of the electrons and holes. Due to these defects and to the presence of deep impurities in the depletion region, the rectifying contact capacitance may be varying. The rectifying devices' traps reduce the free carrier density whereas recombination centers produce generation-recombination current. When the temperature increases, there is a decrease of the built-in potential V_0 and an increase of the carrier concentration N_A (**Figure 6**). This effect may be attributed to the effect of traps [53].

It is known that the depletion layer width, formed in the junction, of the n^+-side of the metal is much smaller than the *p*-side of the semiconductor and can be neglected, and then the layer width W is only reduced to the p-side region and is given by the following expression:

$$W = \left(\frac{2\varepsilon_s V_0}{qN_A}\right)^{1/2} \tag{4}$$

The potential difference V_n between the Fermi level and the top of the valence band in the CIS can be obtained by the following relationship:

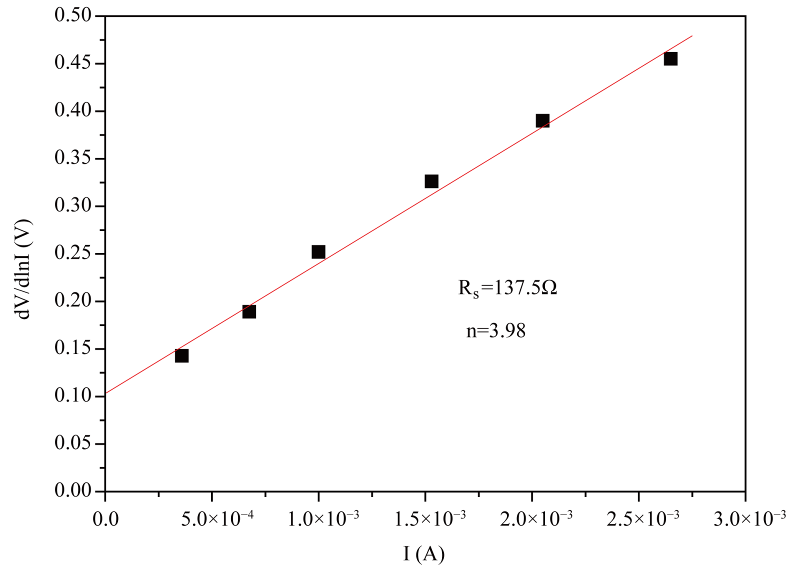

Figure 4. $\frac{\mathrm{d}V}{\mathrm{d}(\ln I)}$ versus the current density at room temperature for Al/p-CIS Schottky junction.

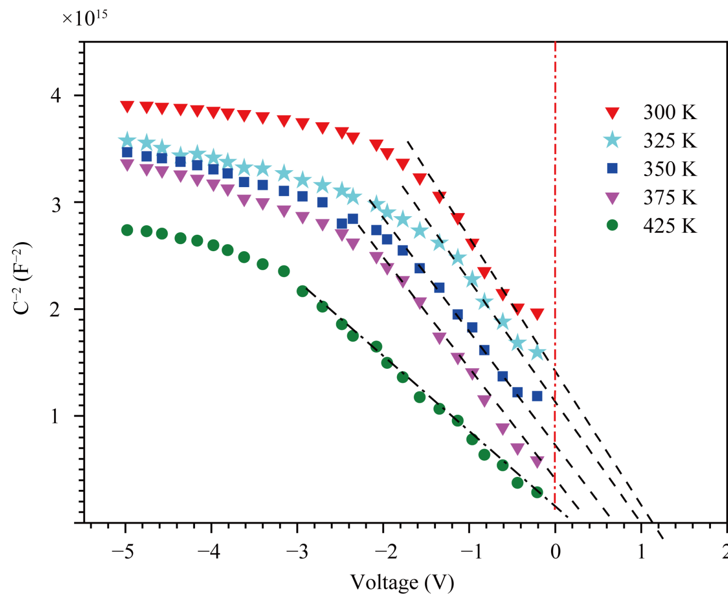

Figure 5. C^{-2}–V of the Al/p-CIS Schottky junction at different temperatures.

$$V_n = \frac{KT}{q}\ln\frac{N_v}{N_A} \tag{5}$$

where N_v is effective density of states in the valence band of the CIS (1.5×10^{19} cm^{-3} [54]).

Thus, the barrier height value for the Al/p-$CuInSe_2$ device is calculated by:

$$\varphi_b = V_0 + V_n \tag{6}$$

Figure 7 shows the variation of the layer width and the barrier height with temperature. We observe that the depletion layer width W decreases with increasing temperature due to the increasing of the carrier density N_A.

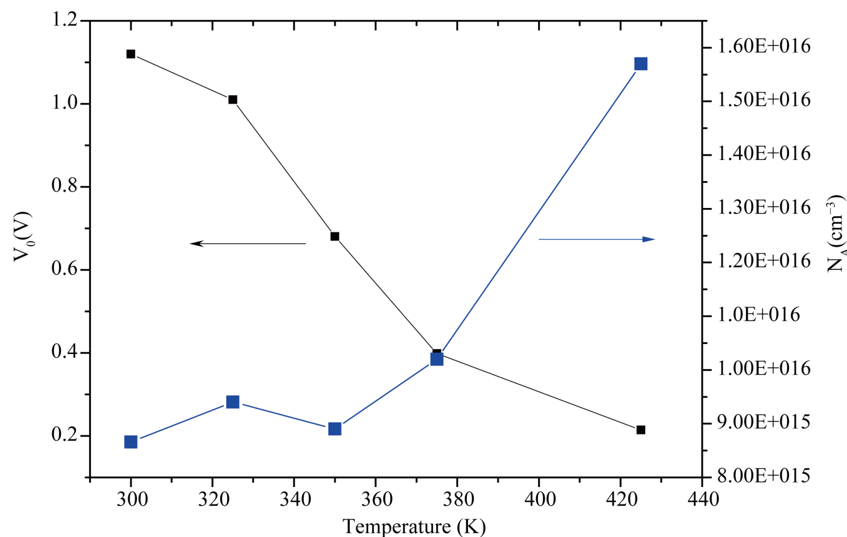

Figure 6. Temperature dependence of V_0 and N_A for the Al/p-CIS Schottky junction.

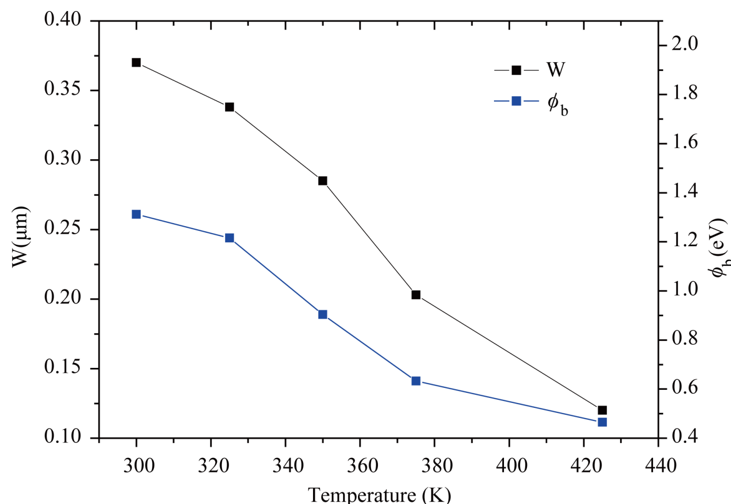

Figure 7. The depletion layer width W and the barrier height φ_b of the Al/p-CIS junction as a function of the temperature.

3.3. Impedance Spectroscopy

The impedance spectra of the Al/p-CIS/FTO heterostructure at zero bias for various temperatures are shown in Figure 8. The electrical response can be fitted as an equivalent AC circuit composed by a single parallel resistor R_p and capacitor C_p network connected to a serial resistor R_s as shown in Figure 9. Its real and imaginary impedance parts Z' and Z'' may be written as:

$$Z' = R_s + \frac{R_p}{1+\omega^2 C^2 R_p^2}, \quad Z'' = \frac{\omega C R_p^2}{1+\omega^2 C^2 R_p^2} \tag{7}$$

The values of the serial resistance R_s and the total resistance $(R_s + R_p)$ are obtained from the low and high frequency intercepts on the Z' axis respectively. The value of the capacitance was found to be slightly frequency dependent. Figure 10 and Figure 11 illustrate the evolution of the equivalent circuit parameters as a function with temperature. It can be observed that all the serial and the parallel resistances and the capacitance decrease with increasing temperature due probably the improvement of the junction structure.

We mention different results for the serial resistance values obtained by the two different methods, from (DC)

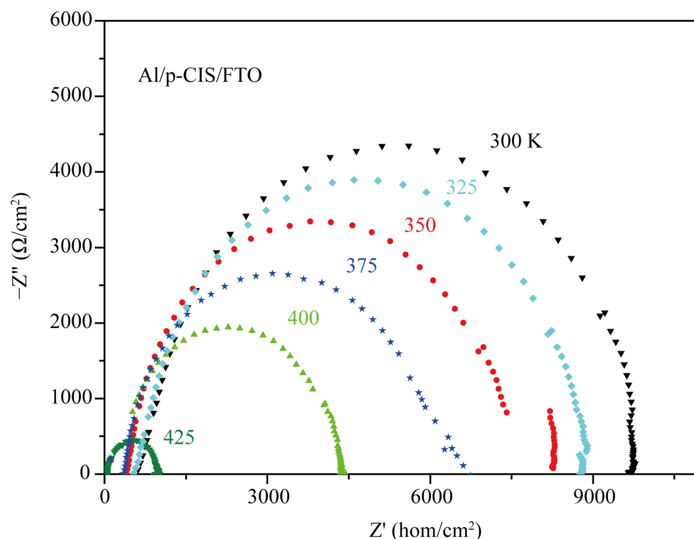

Figure 8. Nyquist diagram of a Al/p-CIS heterojunction at different temperatures.

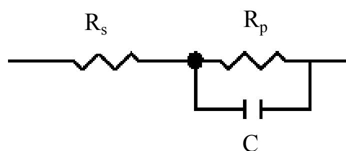

Figure 9. Equivalent circuit for Al/p-CIS Schottky Diode. R_s represents the series resistance, R_p the parallel resistance and C the capacitance.

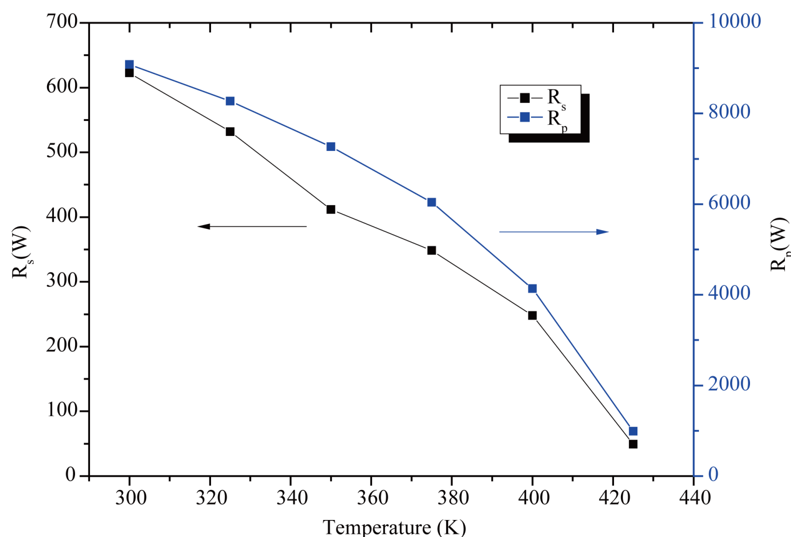

Figure 10. The variation of the series resistance and parallel resistance for different temperatures of Al/p-CIS Schottky diode.

I-V and from (AC) impedancemetry, which are respectively 173.5 Ω and 622.5 Ω at room temperature. The first value is different from the second one and this difference is due to the insufficiency of the conduction model where we don't have take account to the different diffusion processes of the carriers.

In fact, by introducing the previous values of R_s, R_p and C in the theoretical real and imaginary part of the

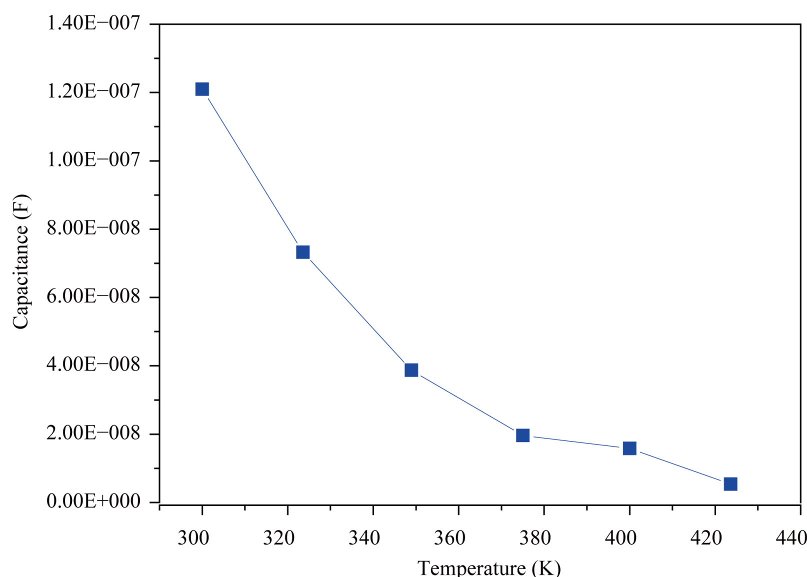

Figure 11. The variation of the space-charge capacitance vs. temperature for Al/p-CIS Schottky Diode.

complex impedance, we have found a good fitting in the range of frequencies 1 kHz to 10 MHz as shown in **Figure 12** for 300 K. This result is also verified for the other chosen temperatures.

When increasing the temperature, the cut-off frequency of the imaginary part of the impedance, shown in **Figure 13**, shifts towards the higher frequencies, and satisfies the theoretical model of the hole traps interacting with the valence band [55]:

$$\omega = A v_{th} \sigma_p N_V \exp - \frac{E_a}{KT} \tag{8}$$

where A is the dimensionless quantity related to the degeneracy factor of the trap and the fixed charge within the depletion region, v_{th} the average thermal velocity of the holes in the valence band, σ_p the capture cross-section of the trap and E_a is the energy difference between the trap level and the valence band. **Figure 14** shows the Arrhenius diagram of the $\ln(\omega)$ versus the inverse of temperature which is linear and proportional to the Activation energy E_a estimated to 0.46 eV.

4. Conclusions

The Al/CIS/FTO heterojunction was fabricated and studied by using I-V, C-V and impedance measurements in the range of temperature 300 K - 425 K. The rectifying behavior confirms that this junction behaves as a Schottky diode with p-type absorber layer. The high value found for the ideality factor is probably due to both the potential drop and the recombination through the interfacial layer. C-V measurements reveal that the carrier concentration of annealed CIS films is in the order of 10^{15} cm^{-3}. In addition, we have observed that the depletion layer width and the barrier height decrease with temperature. We have also given, from the impedance spectra, the electrical equivalent circuit and we have found that their parameters (R_s, R_p and *C*) decrease when annealing temperature increases. Two different results, for the serial resistance R_s, have been deduced from the DC and AC measurements. This difference is due to the insufficiency of the conduction model where we don't have taken into account the different diffusion processes and the existence of trap levels.

The study on temperature of our junction shows some information in transport phenomenon. It shows the quality of the interface between thin layers. Those results are favorable for preparing thin film solar cells with p-CIS as absorber layer. In addition, the electrodeposited absorber layer of $CuInSe_2$ has shown good stability with weak resistance in the interface. Such heterojunction fabrication processes will significantly help the realization of low-cost thin films and this technique may be concurrent to other ones because it is economic, technologically simple and allows the possibility of deposition over large surface areas for the PV solar cells fabrication.

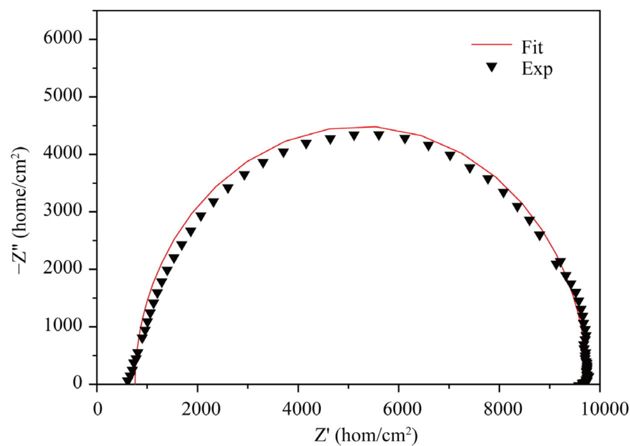

Figure 12. Comparison of the experimental and the theoretical Nyquist diagram at ambient temperature.

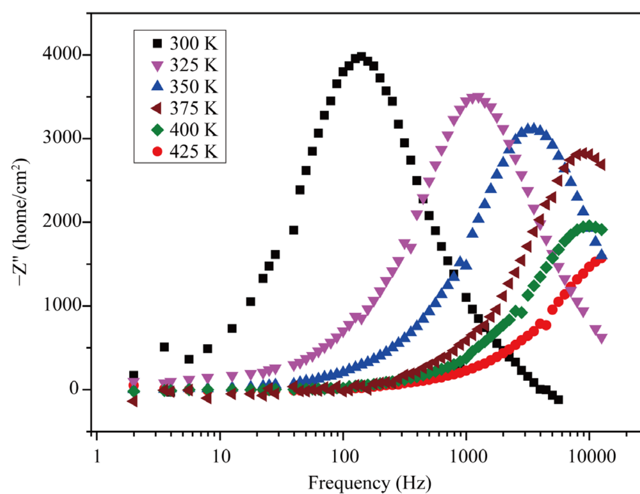

Figure 13. Variation of the cut-off frequency of the imaginary part −Z" at various temperatures.

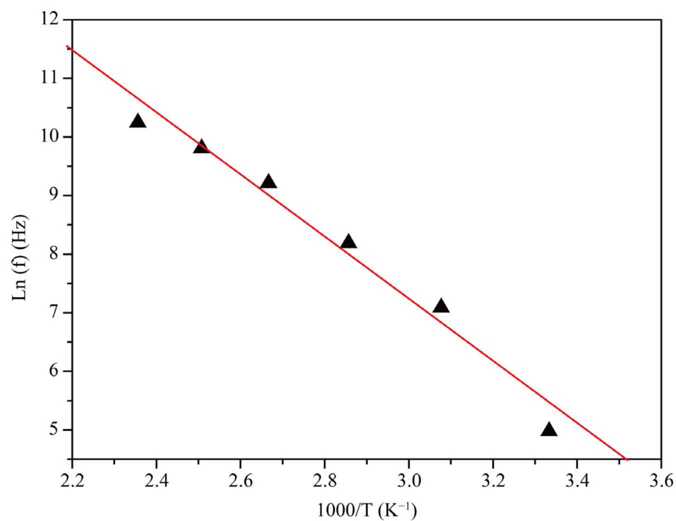

Figure 14. Arrhenius diagram of the cut-off frequency.

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